31st European Symposium
on Reliability of Electron Devices, Failure Physics and Analysis

ESREF 2020

4-8 October 2020
Athens - Greece

Organised by:

https://esref2020.sciencesconf.org/

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IMPORTANT NOTICE

Time schedule is based on the Central European Summer Time Zone (CEST)

ATTENTION: The HOPIN platform will be up and running base on Greek time (Central Europe +1)

CONTENTS

WELCOME TO ESREF 2020

I am pleased and honoured to welcome you to virtual ESREF 2020, the 31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, from October 4 - 8, 2020 in Athens, Greece.

- ESREF allows electronic reliability professionals and failure analysis professionals to meet annually and participate in a rewarding exchange of experience, technical knowledge, and valuable industry connections. This is a rather unique opportunity, which ESREF provides yearly. I have been participating in ESREF from the beginning of my career, and look forward to it every year, as a time to see what is up with the field, exchange news with my colleagues, discuss new challenges, and hopefully find solutions or good hints to solve the new problems we encounter in our daily research. ESREF 2020 will offer something special, giving a particular stress on reliability of power electronics and renewable energy production systems.

This year we have reached the number of 14 technical tracks, including a new topic on batteries, capacitors and passive, for a total of 107 papers spread over 22 oral sessions. Four invited speeches and two papers from the sister conferences ISTFA and IRPS will complete the oral part of the technical session. On top of that, 61 poster papers will be showcased on Monday to Wednesday afternoon, for a total of 171 technical contributions, not to mention the two tutorials on the hot themes of reliability and failure analysis. All the technical papers will be published as a special issue on Elsevier Microeletronics Reliability. This year there will also be a number of industrial presentations in the conference breaks, which I warmly recommend to attend as a unique opportunity to get effectively updated on the state-of-the-art technologies.

I want to make a special mention of the three keynote speeches during the opening session. Trying to match the time difference between the keynote speaker's location:

- The first keynote speech will be given by Dr. Konstantinos Emmanouil, now working with the System Architect, More Electric Engine, Rolls-Royce Deutschland. His talk titled "Reliability in the era of electrification in aviation: a systems approach", which discusses the increasing amount of electrification projects in aviation and the reliability key questions regarding the integration of electric and electronic equipment in areas that have been dominated by thermal machines. The presentation will provide insights into the methods used to determine the required reliability by assessing the whole system and exploring the electromechanical and environmental interactions that define the new requirements to be met.
- The second keynote speech will be given by Prof. Dr. Gabriel Apply, professor of physics at ETH Zürich and EPF Lausanne, and head of the Photon Science Division of the Paul Scherrer Institut. His talk titled **"**High-resolution non-destructive three-dimensional imaging of integrated circuits**".** His speech will focus on the fact that presently semiconductor technology is more advanced in its capacity to create complex systems than in the ability to image the outcomes. The presentation will discuss the impact of conventional high-resolution microscopy for imaging of the interior of three dimensionally structured objects and describe X-ray ptychography, a mixed real space/reciprocal space technique, which is non-destructive and provides three-dimensional images at steadily improving resolution.
- The third keynote speech will be given by Prof. Aristos Christou, Materials Science and Engineering. Mechanical Engineering University of Maryland Energy Innovation Institute Center for Risk and Reliability. His talk is titled "Reliability Limitations from Crystal Defects in Thick GaN Epitacial Layers for Power Electronics". He is a Fellow of the IEEE, a Fullbright Fellow, a recipient of the DoD-Berman Publication Awards, and an IEEE Guest Lecturer. Professor Christou was the recipient of the INEER Achievement Award (International Network for Engineering Education and Research) for achievements in international education and research in engineering, as well as the recipient of the ASM International Burgess Memorial Award "For his seminal scientific contributions in the field of electronic materials, packaging

and devices." In 1986, he established reliability programs in both Italy and Greece. These programs were established under the auspice of the NATO Scientific Affairs Committee for Southern European Stability, a committee in which he was a member. His presentation provides the progress of characterization of thick GaN power semiconductor material epitaxial layers and growth technology, and the potential impact crystal defects may have on high-density power switching electronics. A comparison of the SiC development and manufacturing evolution is made to draw a parallel between SiC and GaN wide bandgap (WBG) semiconductor power electronic.

The technical programme chairs, Prof. Francesco Iannuzzo (Univ. of Aalborg DK), Assoc. Prof. Spyros Gardelis (NKUA, GR), Prof. Philomela Komninou (Auth GR) and Prof. Nikos Melanitis (HNA GR) deserve a special acknowledgment for the hard work done in this edition, comprising, among other things, the full review process of the almost 177 submitted manuscripts with very tight time constraints. My deepest gratitude goes to the 280 reviewers and mentors and the 28 track chairs/Assoc. Editors whom offered for free their expertise to the review process. ESREF 2020 would simply not be happening without their commitment.

Warmest regards,
George Papaioannou
Dept. of Solid St National Kapodistrian University of Athens (NKUA)
ESREF 2020 General chair

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Athens Acropolis Museum

return to contents

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Tracks in ESREF 2020

A - Quality and reliability assessment techniques and methods for devices and systems

- **Ninoslav STOJADINOVIC** - University of Nis, Serbia
- **Edgar OLTHOF** - NXP Semiconductors, Netherlands

B - Failure mechanisms and reliability of micro- and nanoelectronics

- **Alain BRAVAIX** - ISEN-Toulon, France
- **Enrique MIRANDA** - Universitat Autònoma de Barcelona, Spain

C - Progress in failure analysis: defect detection and analysis

- **Ingrid DE WOLF** - IMEC, Belgium
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D - Reliability of microwave devices and circuits

- **Nathalie LABAT** – IMS Bordeaux, France
- **Michael DAMMANN** - Fraunhofer IAF, Germany

E1 - Reliability of die-attach, modules and assemblies

- **Paolo COVA** - University of Parma, Italy

E2 - Solder joint reliability

- **Paolo COVA** - University of Parma, Italy

F1 - Silicon power devices, IGBTs, thyristors

- **Mauro CIAPPA** – ETH Zurich, Switzerland
- **Chiara CORVASCE** - ABB Semiconductors, Switzerland

F2 - Wide-bandgap power devices

- **Matteo MENEGHINI** - University of Padova, Italy
- **Loic THEOLIER** – University of Bordeaux, France

F3 - Power electronic auxiliary circuits and system reliability

- **Francesco IANNUZZO** - Aalborg University, Denmark
- **Hong LI** - Beijing Jiaotong University, China

G - Optoelectronics, Micro-Electro-Mechanical actuators and MEMS

- **Massimo VANZI** - University of Cagliari, Italy
- **Loukas MICHALAS** - FORTH-HELLAS, Greece

H - ESD, EOS, Latch-up, EMC-EMI in integrated and power circuits

- **George PAPAIOANNOU** – University of Athens, Greece

I - Renewable energy systems reliability

- **Haoze LUO** - Zhejiang University, Hangzhou, China
- **Francesco IANNUZZO** - Aalborg University, Denmark

J - Modeling for Reliability

- **Philomela KOMNINOU** – Aristotle University of Thesaloniki, Greece

K - Radiation impact on circuits and systems reliability

- **Francesco IANNUZZO** - Aalborg University, Denmark
- **Nikolaos MELANITIS**, Hellenic Naval Academy, Greece

L – Batteries, capacitors & passives

- **Spyros GARDELIS** - University of Athens, Greece

Athens Acropolis Museum

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We would like to express our gratitude for the generous support received from our technical supporters. ESREF 2020 recognises its supporters as key contributors to the conference.

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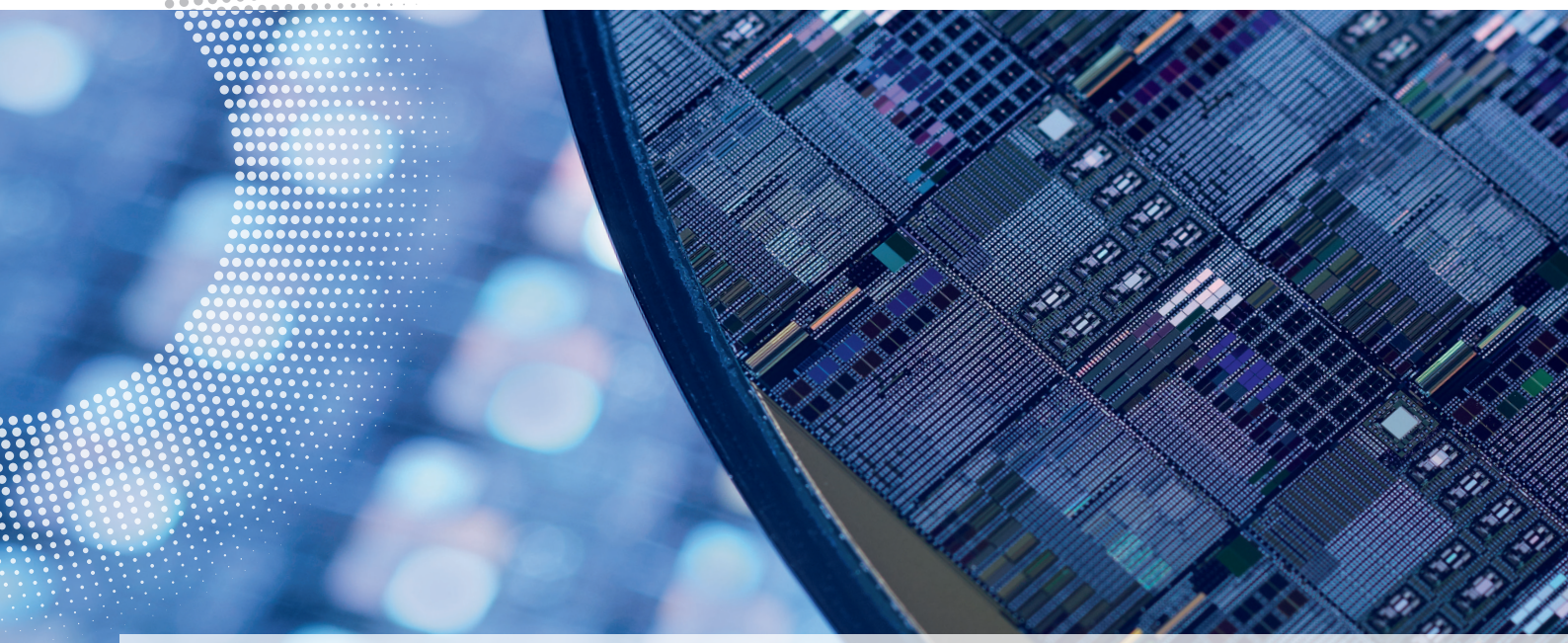

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For more information please contact
Dr. Anne Reiner at areiner@hamamatsu.de

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Booth number: 2

Hitachi Power Solutions develops and provides our original Scanning Acoustic Tomographs and their transducers. Our products' lineup consists of FineSAT series, FS-Line series, Wafer-Line and ES-5100. The FineSAT series can be utilized for non-destructive testing of wide variety of electronic devices and materials not only in laboratories but also in mass-production lines. FS-Line series are optimum for large scale mechanical parts and materials such as sputtering targets. The Wafer-Line is an automated system for bonded Si wafers. ES-5100 can realize extremely high-speed testing on combination with phased array transducers. We can also provide optimum transducers from our wide variety of transducers to customer's samples.

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Booth number: 6

Imina Technologies SA design manufacture and distribute complete lines of robotics solutions for electron and light microscopes. Using a novel mobile motion technology, our robots for microscopes combine nanometer resolution of positioning, unprecedented ease-of-use and flexibility. Their ultra-compact design provides high stability ensuring steady pose over long measurement sequence while preventing sample damages. Our robots can be easily integrated onto optics based investigation tools or inside an SEM for micro- or nano-probing investigations. Overall, this enables FA Engineers to quickly gather data to understand the failure cause.

SECTOR TECHNOLOGIES
Booth number: 8

Sector Technologies is a distributor Company for high-tech products within the European Semiconductor Industry.
Our focus is mainly the distribution of failure analysis high-end equipment. The acceleration of new technology introduction requires new tools for design debug, yield enhancement and customer return. Time to market is key for success and the failure analysis lab is one of the very important bricks of that process. Tools and products must be adapted to the technology challenges but methodology and knowledge are key to the results; this is why we like to say that we provide solutions to our customers. Tools for complex packages failure analysis has become a must, specifically for non-destructive analysis. Lock-in Thermography (Elite), EMMI and laser scanning microscopy application (Meridian family) and nanoprobing (nProber III, Flexprober, Hyperion) from ThermoFisher ; 3D Xray CT (Zeiss Xradia Versa products); Terahertz TDR (EOTPR 2000 from Teraview) are products specifically targeted for process development, yield improvement , failure analysis for complex electronics components.
Samples preparation and backside silicon thinning has also become a significant challenge; varioMill from Varioscale allows outstanding automated backside preparation on single die but also on stacked dies assembly. We also have new products to present in the test and debug area (Mutest, Teseda, Focused Test), test analysissoftware (GAT), probing station (SEMICS).
Our latest partner Nanotronics offers Automated Optical Inspection system for quality and metrology labs,Wafer inspection and Package line inspection.

SMARACT GMBH

Booth number: 13

We at SmarAct develop, produce and distribute piezo-based high-performance micro- and nanopositioners, advanced control systems and micro-tools. Furthermore, we manufacture complete miniaturized manipulation systems, ranging from single linear axes and rotary positioners to XY tables and compact 6D manipulators to multi-manipulator systems. Our microscopy products, which can be applied in normal pressure as well as in vacuum conditions, are used in a wide range of industries. Our customers benefit from our over 10 years of experience in several scientific fields. This, accompanied by the entire value-added chain of development, production, distribution and a professional service, enables us to react fast to almost any of your demands, when it comes to customization and complexity.

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Booth number: 14

The John P. Kummer Group has served as a specialist distributor of instruments, used in the manufacturing of semiconductors, for several decades. Taking advantage of our long established relationships within the worldwide Industry, we bring the newest and most technologically advanced products to the European Microelectronics Community. The focus of John P. Kummer Group combines equipment for failure analysis, reliability testing and process tools as well as specialty adhesives for use in advanced technology applications. The fields of product applications are various as semiconductor, hybrids microelectronics, circuit/electronic assembly, medical devices and optical materials.

MATERIALS ANALYSIS TECHNOLOGY INC.

Booth number: 19

Materials Analysis Technology Inc. (MA-tek) is a world-class laboratory providing services in materials analysis (MA). In line with the exponential rate of the business's development, MA-tek has successfully expanded to be equipped with additional Failure Analysis (FA) and Reliability Testing (RT) services. These integrations allow for MA-tek to provide superior service for its customers in various industries. MA-tek currently has 7 laboratories and 1 sales office set up around the world, providing around-the-clock assistance in logistic support and technical services.

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return to contents

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return to contents

GENERAL INFORMATION

The ESREF2020 will be hosted in a virtual environment supported by Boussias Communications in a virtual platform. The platform will be available 24 hours a day for the whole duration of the conference where you can visit sessions, networking and exhibitors' booths.

INFORMATION FOR PRESENTERS

Oral Presentations

The time slot for Tutorials is 90 min, for Keynotes 40 + 5 min, Invited 25 + 5 min and oral is 15 + 5 min (the 5 minutes are allocated for questions).
Presenters should be aware of the date, session, room, time & number of their presentation since each session will be assigned a separate room corresponding to the 3 parallel sessions. Presenters MUST be very accurate with the time schedule that they are assigned in the programme and be ready to share their screen and proceed with their presentation according to the instructions and demo guided by Boussias Communications.

Poster Presentations

Each poster presenter will be assigned a presentation room (under sessions) and he will be the sole moderator of his poster for one and a half hours (1hr 30 min) according to the announced programme.
Each poster is assigned a unique code, and must have only one presenter, the name of which will be used to open the communication room. The presenter will have the role of a moderator, thus, he will have full access to present his poster (maximum 3 slides) and handle Q&A during the poster presentation utilising any possible additional slides he might need to display in supporting his research work.

PROGRAMME

Sunday, October 4

Stage (Room for All)

Tutorials

Chair: Philomela Komninou

09:00 **Elke Meissner**
T1 *Defects and performance of devices on G*

10:30 **Break**

10:45 **Tetsu Kachi**
T2 *Vertical GaN devices and reliability*

12:15 **Break**

Stage (Room for All)

ESREF 2020 Opening

12:30 **George Papaioannou**
Opening remarks

Stage (Room for All)

Keynotes

Chair: George Papaioannou

12:50 **Konstantinos Emmanouil**
KN1 *Reliability in the era of electrification in aviation: a systems approach*

13:35 **Break**

14:00 **Gabriel Aeppli**
KN2 *High-resolution non-destructive three-dimensional imaging of integrated circuits*

14:45 **Aris Christou**
KN3 *Reliability limitations from crystal defects in Thick GaN epitaxial layers for Power Electronics*

Monday, October 5

Room A

Session aA1 - Quality and reliability assessment techniques and methods for devices and systems

Chairs: N. Stojadinovic, E. Olthof

09:00 **Kai Xi,** Jinshun Bi
31 ***Impact of electrical stress on total ionizing dose effects on graphene nano-disc non-volatile memory devices***

09:20 **Mingyue Liu,** Hao Cai, Yongliang Zhou, Bo Liu and Lirida
142 ***CSME: A novel cycle-sensing margin enhancement scheme for high yield STT-MRAM***

09:40 **Yongliang Zhou**, Hao Cai, Mengdi Zhang, Lirida Naviner and Jun Yang
135 ***A Novel BIST for monitoring aging /temperature by self triggered scheme to improve the reliability of STT-MRAM***

10:00 **Markus Sievers**, Bettina Findenig,Michael Glavanovics, Thomas Aichinger and Bernd Deutschmann
129 ***Monitoring of parameter stability of SiC MOSFETs in real application tests***

10:20 Shu-Han Hsu, Ying-Yuan Huang, Yi-da Wu, Kexin Yang, Li-Hsiang Lin and **Linda Milor**
176 ***Extraction of wearout model parameters using on-line test of an SRAM***

Room B

Session bF1 - Silicon power devices, IGBTs, thyristors

Chairs: M. Ciappa, C. Corvasce

09:00 **Nausicaa Dornic,** Ali Ibrahim, Zoubir Khatir, Nicolas Degrenne, Stefan Mollov and Damien Ingrosso
137 ***Analysis of the aging mechanism occurring at the bond-wire contact of IGBT power devices during power cycling***

09:20 **Koichi Endo,** Norimichi Chinone, Tomonori Nakamura, Toru Matsumoto and Koji Nakamae
141 ***Single-pulse observation of photoemission during avalanche breakdown in insulated gate bipolar transistor***

09:40 **Metayrek Youssef,** Kociniewski Thierry, Khatir Zoubir
149 ***Thermal behaviour evolution of an IGBT chip after aging measured by thermoreflectance***

10:00 **Kazunori Hasegawa,** Seiya Abe, Masanori Tsukuda, Ichiro Omura and Tamotsu Ninomiya
199 ***Shoot-through protection for an inverter consisting of the next-generation IGBTs with gate impedance reduction***

10:20 **Konstantinos Patmanidis**, Michael Glavanovics, Angelos Georgakas and Annette Muetze
113 ***Modular dynamic pulse stress test system for discrete high power semiconductors***

Room C

Session cF2-1 - Wide bandgap power Devices: SiC and Ga2O3 device reliability

Chairs: L. Theolier

09:00 **Mauro Ciappa**, and Marco Pocaterra

138 ***On the use of soft gamma radiation to characterize the pre-breakdown carrier multiplication in SiC power MOSFETs and its correlation to the TCR failure rate as measured by neutron irradiation***

09:20 **Cyril Buttay**, Hiu-Yung Wong, Boyan Wang, Ming Xiao, Christina DiMarino and Yuhao Zhang

104 ***Surge current capability of ultra-wide-bandgap Ga2O3 schottky diodes***

09:40 **Giovanni Susinni**, Francesco Iannuzzo, Angelo Raciti, Santi Agatino Rizzo

260 ***A non-invasive SiC MOSFET junction temperature estimation method based on the transient light emission from the intrinsic body diode***

10:00 **Alberto Castellazzi**, Frédéric Richardeau, Alessandro Borghese, Francois Boige, Asad Fayyaz, Andrea Irace, Gerald Guibaud, and Vanessa Chazal

243 **Gate-damage accumulation and off-line recovery in SiC power MOSFETs with soft short-circuit failure mode**

Invited talk

10:20 **Alberto Castellazzi**

INV1 ***Fail-to-open short-circuit failure mode in SiC power MOSFETs, device characterization and system level exploitation***

10:50 Break

Room A

Session aE1 - Reliability of die-attach, modules and assemblies

Chairs: P. Cova

11:10 Paolo Cova, **Danilo Santoro,** Davide Spaggiari, Federico Portesine, Filippo Vaccaro, Nicola Delmonte

228 ***CFD modelling of additive manufacturing liquid cold plates for more reliable power press-pack assemblies***

11:30 **Ciro Scognamillo**, Antonio Pio Catalano, Philippe Lasserre, Cyrille Duchesne, Vincenzo d'Alessandro, Alberto Castellazzi

110 ***Combined Experimental-FEM Investigation of electrical ruggedness in double-sided cooled power modules***

11:50 **Le Xu,** Sanqiang Ling, Donghui Li , Guofu Zhai

52 ***Vibration-induced dynamic characteristics modeling of electrical contact resistance for connectors***

12:10 **Elisabeth Kolbinger,** Simon Kuttler, Stefan Wagner, Martin Schneider-Ramelow

98 ***Investigation of the mechanical properties of corroded sintered silver layers by using Nanoindentation***

12:30 Amina Tablati, Nadim Alayli, Toni Youssef , Olivier Belnoue, **Loic Théolier,** Eric Woirgard
225 ***New power module concept in PCB-Embedded technology with silver sintering die attach***

Invited talk

12:50 **Nicola Delmonte**
INV2 ***3D and compact thermal modeling in power electronics: an overview***

Room B

Session bC - Progress in failure analysis - defect detection and analysis

Chairs: I. de Wolf, F. Altmann

11:10 Isaak G. Vasileiadis, Imad Belabbas, Joanna Moneta, Julita Smalc-Koziorowska, Philomela Komninou, **George P. Dimitrakopulos**
262 ***Radiation-enhanced glide of 30o Shockley partial dislocations in gallium nitride heterostructures***

11:30 Jun Hirota, Kohei Yamasue, **Yasuo Cho**
17 ***Profiling of carriers in a 3D flash memory cell with nanometer-level resolution using scanning nonlinear dielectric microscopy***

11:50 **Hideo Tanaka**, Chun-Cheng Tsao
177 ***Reliable endpoint technique on si trenching for backside circuit edit***

12:10 **Ingrid De Wolf,** Kristof J.P. Jacobs, Antonio Orozco
188 ***Magnetic field imaging and light induced capacitance alteration for failure analysis of Cu-TSVinterconnects***

12:30 **Tommaso Melis**, Emmanuel Simeu, Etienne Auvray, Paul Armagnat
56 ***Analog and mixed-signal circuits simulation for product level EMMI analysis***

12:50 **Michael Hertl,** Florie Mialhe, Isaline Richard
139 ***On the replacement of water as coupling medium in scanning acoustic microscopy analysis of sensitive electronics components***

Room C

Session cB – Failure mechanisms and reliability of micro- and nanoelectronics

Chairs: A. Bravaix, E. A. Miranda

11:10 **Michael Waltl,** Bernhard Stampfer, Gerhard Rzepa, Ben Kaczer, Tibor Grasser
171 ***A Single-Trap Study of PBTI in SiON nMOS transistors***

11:30 **Giusy Lama,** Guillaume Bourgeois, Mathieu Bernard, Niccolo Castellani, Jury Sandrini, Emmanuel Nolot, Julien Garrione, Marie Claire Cyrille, Gabriele Navarro, Etienne Nowak
217 ***Reliability analysis in GeTe and GeSbTe based phase-change memory 4kb arrays targeting storage class memory applications***

11:50 Shuang Li, **Alain Bravaix,** Edith Kussener, David Ney, Xavier Federspiel, Florian Cacho
223 ***Hot-carrier degradation in P- and N- channel EDMOS for smart power application***

12:10 Junjun Zhang, **Fanyu Liu,** Bo Li, Binhong Li, Yang Huang, Can Yang , Guoqing Wang , Rongwei Wang, Jiajun Luo, Zhengsheng Han
220 ***Single event upset for monolithic 3-D integrated 6T SRAM based on a 22 nm FD-SOI technology: Effects of channel size and temperature***

12:30 **Rafael Nunes**, José Ramirez, Roberto Orio
246 ***Methodology to evaluate the critical blocks in an integrated circuit based on the temperature***

12:50 Jordi Muñoz Gorriz, Mireia Gonzalez, Francesca Campabadal, Jordi Suñe, **Enrique Miranda**
106 ***Analysis of the successive breakdown statistics of multilayer Al2O3/HfO2 gate stacks using the time-dependent clustering model***

13:10 **Debao Wei,** Hua Feng, Xiaoyu Chen, Liyan Qiao and Xiyuan Peng, Harbin Institute of Technology
91 ***Research on 3D NAND flash reliability from the perspective of threshold voltage distribution***

13:30 Break

Poster Room

14:00 -15:30 Poster Session 1

1a: A - Quality and reliability assessment techniques and methods for devices and systems

8 Seung Hyun Kim, **Si-Il Sung**
Modeling and analysis of the catastrophic failure and degradation data

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15 **Guangze Pan**, Yaqiu Li, Xiaobing Li, Qin Luo, Chunhui Wang, Xianghong Hu
A reliability evaluation method for multi-performance degradation products based on the Wiener process and Copula function

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28 **Shu-Han Hsu,** Ying-Yuan Huang, Yi-da Wu, Kexin Yang, Li-Hsiang Lin and Linda Milor ***Optimal sampling for accelerated testing in 14nm FinFET ring oscillators***

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90 **Xuerong Ye,** Hao Chen, Qisen Sun, Cen Chen, Hao Niu, Guofu Zhai, Wenwen Li, Ruiming Yuan
Life-cycle reliability design optimization of high-power dc electromagnet-ic devices based on time-dependent non-probabilistic convex model pro-cess

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93 Debao Wei, Xiaoyu Chen, **Hua Feng,** Liyan Qiao, Xiyuan Peng
A high-efficiency threshold voltage distribution test method based on the reliability of 3D NAND flash memory

132 **Yaqiu Li,** Guangze Pan, Qian Li, Chunhui Wang and Xianghong Hu
A novel accelerated life-test method under thermal cyclic loadings for electronic devices considering multiple failure mechanisms

160 **Pan Yang,** Xiaocan Ye, Yongxin Zhao, Wei Zhang, Shoumou Huang, Yang Huang, Yujie Wang
An error detecting scheme with input offset regulation for enhancing reliability of ultralow-voltage SRAM

178 Debao Wei**, Zhelong Piao,** Hua Feng, Liyan Qiao, Xiyuan Peng
FPGA-based reliability testing and analysis for 3D NAND flash memory

182 **Muhammad Waqar,** Sanghyeon Baeg, Geunyong Bak, Junhyeong Kwon, Kiseok Lee and Sang Hoon Jeon
FBGA solder ball defect effect on DDR4 data signal rise time and ISI measured by loading the data line with a capacitor

190 Yongquan Sun, **Jiaying Guo,** Jia Qi, Bo Liu and Tianhua Yu
Comparisons of SnO2 Gas sensor degradation under elevated storage and working conditions

212 **Yasmin Abdul Wahab,** Mohd Rafie Johan, Nor Aliya Hamizi, Omid Akbarzadeh, Zaira Zaman Chowdhury, Suresh Sagadevan
Effect of integrated anneal optimizations of electroplated Cu thin films Interconnects

230 **Giovanna Mura,** Roberto Murru, Giovanni Martines
Analysis of counterfeit electronics

248 **Ankush Oberai**, Rupa Kamoji
Smart manufacturing through predictive FA

264 **Sze Li Harry Lim,** Pham Luu Trung Duong, Hyunseok Park, Preetpal Singh, Cher Ming Tan and Nagarajan Raghavan
Assessing multi-output gaussian process regression for modeling of non-monotonic degradation trends of light emitting diodes in storage

1b: I - Renewable energy systems reliability

222 **Peng Fan**, Shoudao Huang, Derong Luo
Electro-thermal evaluation and comparison of quasi-z source inverter using different modulation methods in wind power system

1c: K -Radiation impact on circuits and systems reliability

36 **Xiuhai Cui**, Liansheng Liu
Mitigating single event upset of FPGA for the onboard bus control of satellite

42 **Ygor Q. Aguiar,** Frédéric Wrobel, Jean-Luc Autran, Paul Leroux, Frédéric Sagné, Vincent Pouget and Antoine Touboul
Reliability-driven pin assingment optimization to improve in-orbit soft-error rate

181 **Jiantou Gao**, Cai Li, Binhong Li, Bo Li, Fazhan Zhao, Jing Li, Gang Zhang, Chunlin Wang, Chuanbin Zeng, Jie Liu, Shuai Cui, Qinzhi Wu and Tianchun Ye
Single-event induced failure mode of PWM in DC/DC converter

201 **Ygor Q. Aguiar**, Frédéric Wrobel, Jean-Luc Autran, Paul Leroux, Frédéric Sagné, Vincent Pouget, Antoine Touboul
Design exploration of majority voter architectures based on the signal probability for TMR strategy optimization in space applications

203 **Corrado De Sio,** Sarah Azimi, Luca Sterpone
On the Analysis of radiation-induced Failures in the AXI Interconnect Module

207 German Leon, Jose M. Badia, **Jose A. Belloch**, Almudena Lindoso and Luis Entrena
Evaluating the soft error sensitivity of a GPU-based SoC for matrix multiplication

213 **Dongqing Li,** Tianqi Liu, Zhenyu Wu, Chang Cai, Peixiong Zhao, Ze He and Jie Liu
An Investigation of FinFET single-event latch-up characteristic and mitigation method

237 **Rafael Schvittz,** Ygor Quadros Aguiar, Frédéric Wrobel, Jean-Luc Autran, Leomar Rosa Jr, Paulo F. Butzen
Comparing analytical and monte-carlo-based simulation methods for logic gates SET sensitivity evaluation

Tuesday, October 6

Room A

Session D – Reliability of microwave devices and circuits

Chairs: M. Dammann, N. Labat

9:00 **Jean-Guy Tartarin,** Oana Lazar, Alexandre Rumeau, Bernard Franc, Laurent Bary, Benoit Lambert
40 ***Analysis of drain current transient stability of AlGaN/GaN HEMT stressed under HTOL & HTRB, by random telegraph noise and low frequency noise characterizations***

9:20 **Jerome Van de Casteele**, Hannes Stuhldreier, Diane Bouw, Cyril Gourdon, Marianne Raoult, Erwan Durand, Sebastien Van Den Berghe, Marc Hollmer, Marco Grunwald, Benoit Lambert, Herve Blanck, Andrew Barnes
82 ***0.5µm GaN RF power bar technology space evaluation***

9:40 **Elsa Pérez-Martín,** Daniel Vaquero,Hector Sánchez-Martín, Christophe Gaquière, Victor Javier Raposo, Tomás González, Javier Mateos, Ignacio Iñiguez-de-la-Torre
170 ***Analysis of trap states in AlGaN/GaN self-switching diodes via impedance measurements***

10:00 Sebastián Matías Pazos,Fernando Leonel Aguirre,Félix Palumbo, **Fernando Silveira**
202 ***Hot-carrier-injection resilient RF power amplifier using adaptive bias***

10:20 **Zhan Gao**, Fabiana Rampazzo, Matteo Meneghini, Carlo De Santi, Francesca Chiocchetta, Daniele Marcon, Gaudenzio Meneghesso and Enrico Zanoni
259 ***Degradation mechanism of 0.15 um AlGaN/GaN HETMs: the effects of hot electrons***

Room B

Session I - Renewable energy systems reliability

Chairs: H. Luo, F. Iannuzzo

9:00 **Ping Liu**, Jie Xu and Chunming Tu
65 *Thermal Optimized Discontinuous Modulation Strategy for Three Phase Impedance Source Inverter*

9:20 **Shuaichen Ye**, Dao Zhou and Frede Blaabjerg
123 *System-level Reliability Assessment for a Direct-drive PMSG Based Wind Turbine with Multiple Converters*

9:40 **Qingqing Yang,** Rui Wang, Mingyao Ma, Shuying Yang and Xing Zhang
92 *A fault tolerant switched reluctance motor drive for electric vehicles under multi-switches open- fault conditions*

10:00 **Dingyi Wang**, Haoran Wang and Xing Zhang
151 *Mission profile-oriented configuration of PV panels for lifetime and cost-efficiency of PV inverters*

10:20 **Wonwook Oh,** Hoonjoo Choi, Kun Won Seo, Haeseok Lee, Donghwan Kim, Daesung Kim, So-Yeon Kim, Heon Hwang
4 *PV system performance and failure evaluation of 10 year field-aged 1-MW PV power plant*

10:40 Break

Room A

Session aA2 - Quality and reliability assessment techniques and methods for devices and systems

Chairs: Ninoslav Stojadinovic, Edgar Olthof

11:00 **Jiaxin Yuan**, Sujuan Zhang, Bo Wan, Guicui Fu and Maogong Jiang
53 *Damage based PoF model of solder joints under temperature cycling and electric coupling condition*

11:20 **Sanqiang Ling,** Le Xu, Donghui Li and Guofu Zhai
44 *Fretting wear reliability assessment methodology of gold-plated electrical connectors considering manufacture parameters distribution*

11:40 **Martin B. Fogsgaard**, Francesco Iannuzzo
166 *FEM-aided damage model calibration method for experimental results*

12:00 Xuerong Ye**, Hao Chen,** Yue Wang, Hao Niu, Guofu Zhai, Wenwen Li and Ruiming Yuan
41 *Solving time-dependent reliability-based design optimization by adaptive differential evolution algorithm and time-dependent polynomial chaos expansions(ADE-T-PCE)*

12:20 **Alexandra Lackmann Zimpeck,** Cristina Meinhardt, Laurent Artola, Guillaume Hubert, Fernanda Kastensmidt and Ricardo Reis

155 ***Circuit Design using Schmitt Trigger to Reliability Improvement***

Room B

Session bE2 - Solder joint reliability

Chairs: Paolo Cova

11:00 Faical Arabi, Alexandrine Gracia, Jean-Yves Delétage and Helene Fremont

81 ***Effect of Thermal and Vibrational Combined Ageing on QFN Terminal Pads Solder Reliability***

11:20 **Faical Arabi**, Toni Youssef, Martin Coudert, Gérard Coquery, Nadim Alayli, Donatien Martineau and Olivier Belnoue

115 ***Thermo-Mechanical Assessment of Silver Sintering for Attaching Power Components in Embedded PCB***

11:40 Agnieszka Betzwar, Martin Lederer and **Golta Khatibi**

172 ***A lifetime assessment and prediction method for large area solder joints***

12:00 **Charalampos Papadopoulos,** Marta Cammarata, Jan Prinz, Consolato Morabito, Thomas Villiger, Sebastian Steiner, Andy Rodriguez, Jaedoo Kwon, Joerg Krinke, Juergen Urban, Heidrun Kabus, Rolf Geilenkäuser, Jens Dienelt, Dirk Breuer and Frank Kuechenmeister

154 ***Gold Wire Bond Study for Automotive Application***

12:20 **Yuxiong Pan,** Guifa Zhou, Xu Wang and Fen Kuang

62 ***A rapid life-prediction approach for solder joints based on modified Engelmaier fatigue model***

Room C

Session cG1 - Photonics

Chairs: Massimo Vanzi , Loukas Michalas

11:00 Matteo Bertoncello, Fabio Casulli, Marco Barbato, Elisa Artegiani, Alessandro Romeo, Nicola Trivellin, Enrico Zanoni, **Matteo Meneghini** and Gaudenzio Meneghesso

158 ***Influence of copper and CdTe thickness in the reliability of CdS/CdTe solar cells***

11:20 **Francesco Piva,** Carlo De Santi, Matteo Buffolo, Mattia Taffarel, Gaudenzio Meneghesso, Enrico Zanoni and Matteo Meneghini

206 ***Degradation mechanisms in high power InGaN semiconductor lasers investigated by electrical, optical, spectral and C-DLTS measurements***

11:40 **Alessandro Caria,** Carlo De Santi, Filippo Zamperetti, Xuanqi Huang, Houqiang Fu, Hong Chen, Yuji Zhao, Andrea Neviani, Gaudenzio Meneghesso, Enrico Zanoni and Matteo Meneghini

224 ***GaN-based high-periodicity multiple quantum well solar cells: degradation under optical and electrical stress***

12:00 **Marco Simonazzi,** Giovanni Chiorboli, Paolo Cova, Roberto Menozzi, Danilo Santoro, Sergio Sapienza, Corrado Sciancalepore, Giovanna Sozzi and Nicola Delmonte

167 ***Smart Soiling Sensor for PV Modules***

12:20 Mingyao Ma, **Zhixiang Zhang,** Heng Liu, Ping Yun, Xing Zhang and Fei Li

22 ***Fault diagnosis of cracks in crystalline silicon photovoltaic modules through I-V curve***

12:40 Break

Stage (Room for All)

Industrial 1 - Imina Technologies SA

13:40 **Karl Boche**

IND1 ***Electrical nanoprobing and EBIC/EBAC technique integrated in your EFA workflow***

Poster Room

14:00 -15:30 Poster Session 2

2a: F1 - Silicon power devices, IGBTs, thyristors

9 **Yoshiro Baba** and Ichiro Omura

Effect of the cell size reduction on the threshold voltage of UMOSFETs

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29 **Yoann Buvat**, Emilien Bouyssou, Benjamin Morillon and Gaël Gautier

Ageing of glass passivated TRIAC devices under thermal and electrical stress

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231 **Wanping Li,** Bixuan Wang, Jingcun Liu, Guogang Zhang and Jianhua Wang

IGBT Aging Monitoring and Remaining Lifetime Prediction Based on Long Short-Term Memory (LSTM) Networks

2b: F2 - Wide bandgap power Devices

18 **Kohei Yamasue** and Yasuo Cho

Spatial scale dependent impact of non-uniform interface defect distribution on field effect mobility in SiC MOSFETs

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102 **Bixuan Wang,** Jingcun Liu, Wanping Li, Guogang Zhang, Yingsan Geng and Jianhua Wang

Multiple Failure Modes Identification of SiC planar MOSFETs in Short-circuit Operation

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108 Cheng Chen, **Tien Anh Nguyen,** Denis Labrousse, Stéphane Lefebvre, Cyril Buttay and Hervé Morel

New definition of critical energy for SiC MOSFET robustness under short circuit operations: the repetitive critical energy

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159 **Yasin Gunaydin**, Saeed Jahdi, Olayiwola Alatise, Jose Ortiz Gonzalez, Avinash Aithal, Xibo Yuan and Phil Mellor

Analysis of cyclic spontaneous switchings in GaN & SiC cascodes by snappy turn-off currents

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174 Sunday Nereus Agbo, **Jose Ortiz Gonzalez,** Ruizhu Wu, Saeed Jahdi and Olayiwola Alatise

UIS performance and ruggedness of stand-alone and cascode SiC JFETs

189 **Kazuhiro Chou,** Takanori Isobe and Tomoyuki Mannen
Impact of stray-inductance imbalance on short-circuit capability of multi-chip SiC power modules

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214 **He Du,** Sebastian Letz, Nick Baker, Thomas Goetz, Francesco Iannuzzo and Andreas Schletz
Effect of short-circuit degradation on the remaining useful lifetime of SiC MOSFETs and its failure analysis

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221 **Carlo De Santi,** Luca Pavanello, Arianna Nardo, Claudio Verona, Gianluca Verona Rinati, Gaudenzio Meneghesso, Enrico Zanoni and Matteo Meneghini
Reliability of H-terminated diamond MESFETs in high power dissipation operating condition

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241 **Taichi Nakayama,** Tomoyuki Mannen, Akira Nakajima and Takanori Isobe
Gate threshold voltage instability and on-resistance degradation under reverse current conduction stress on e-mode gan-hemts

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251 **Samaneh Sharbati,** Thomas Ebel and Wulf-Toke Franke
Design of E-Mode GaN HEMTs by the Polarization Super Junction (PSJ) Technology

2c: F3- Power electronic auxiliary circuits and system reliability

23 Mingyao Ma, **Xuesong Yan,** Weisheng Guo, Shuying Yang, Guoqing Cai and Wenjie Chen
Online junction temperature estimation using integrated NTC thermistor in IGBT modules for PMSM drives

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27 **Qingqing Yang,** Mingyao Ma, Shuying Yang and Xing Zhang
An active thermal management strategy for switched reluctance drive system with minimizing current sampling delay

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38 Guoliang Yang, **Jinze Yin**, Zhiying Huang and Yuna Zhang
Three-level inverters improve reliability based on equivalent input disturbance and repetitive control combinations

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70 **Puyu Wang,** Song Wang, Xiao-Ping Zhang, Xin Zhao and Zhengrong Xiang
Simplified hybrid reliability simulation approach of a VSC DC Grid with Integration of an improved DC current flow controller

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97 **Qiuling Cao,** Yanbo Che, Jianxiong Yang and Menglai Mi
Short-circuit and open-circuit faults monitoring of IGBTs in SST using collector-emitter voltage

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134 **Taro Takamori,** Keiji Wada, Wataru Saito and Shin-ichi Nishizawa
Gate drive circuit for current balancing of parallel-connected SiC-JFETs under avalanche mode

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136 Xiaofeng Yang, **Jingda Gu,** Trillion Q. Zheng and Zhijun Zhao
Faults and reliability analysis of negative resistance converter traction power system

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164 **Xiaofu Fan,** Dongyuan Qiu, Bo Zhang, Yanfeng Chen, Runhong Huang, Wanyu Cao, Shukai Xu, Chuang Fu, Hong Rao and Licheng Li
Mode identification for reliability improvement of MMC

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208 **Shin-Ichiro Hayashi** and Keiji Wada
Accelerated aging test for gate oxide degradation in SiC MOSFETs for condition monitoring

215 Hong Li, **Xiaheng Jiang,** Ying Zou, Chen Liu
A time-domain stability analysis method for paralleled LLC resonant converter system based on floquet theory

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245 **Tomoyuki Mannen,** Takanori Isobe, Keiji Wada
Investigation of multiple short-circuits characteristics and reliability in SiC power devices used for a start-up method of power converters

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257 **Afshin Loghmani Moghaddam Toussi,** Amir Sajjad Bahman, Francesco Iannuzzo, and Frede Blaabjerg
Parameters sensitivity analysis of Silicon Carbide buck converters to extract features for condition monitoring

Wednesday, October 7

Room A

Session aJ: Modeling for Reliability

Chairs: P. Komninou

09:00 **Romit Kulkarni,** Mahdi Soltani, Simon Krafft, Tobias Groezinger and André Zimmermann
107 ***Coupled simulations for lifetime prediction of board level packages encapsulated by thermoset injection moulding based on the Coffin-Manson relation***

09:20 **Emna Ben Romdhane,** Alexandrine Guédon-Gracia, Samuel Pin, Pierre Roumanille and Hélène Frémont
229 ***Impact of crystalline orientation of lead-free solder joints on thermomechanical response and reliability of ball grid array components***

09:40 **Ionut Vernica,** Ui-Min Choi, Huai Wang and Frede Blaabjerg
144 ***Wear-out failure of an igbt module in motor drives due to uneven thermal impedance of power semiconductor devices***

10:00 **Xiaotong Zhang**, Shihang Wang, Lei Xin, Kangning Wu, Xiaoling Yu, Xiaolin Wang and Jianying Li
194 ***A 3-D thermal network model for the temperature monitoring of thermal grease as interface material***

10:20 **Tatsuya Ohguro,** Yuki Yagi and Yukiko Kashiura
32 ***Study of temperature dependence of breakdown voltage and AC TDDB reliability for thick insulator film deposited by plasma process***

Room B

Session bF3 - Power electronic auxiliary circuits and system reliability

Chairs: H. Li, F. Iannuzzo

09:00 **Kaichen Zhang,** Gerd Schlottig, Elena Mengotti, Francesco Iannuzzo and Olivier Quittard.
263 ***Study of moisture transport in silicone gel for IGBT modules***

09:20 **Hong Li,** Ying Zou, Xiaheng Jiang and Chen Liu
117 ***A time-domain stability analysis method for LLC resonant converter based on Floquet theory***

09:40 **Jianwei Yang,** Zhiyong Dai and Zhen Zhang
14 ***Modeling and fault diagnosis of multi-phase winding inter-turn short circuit for five-phase PMSM based on Improved trust region***

10:00 **Felix Hoffmann,** Sarah Rugen, Dieter Silber and Nando Kaminski
12 ***Impact of sensing current density on PN-Junction based temperature estimation methods for Si and SiC power devices***

10:20 **Yiyan Lu,** Zhao Liu, Jianshou Kong and Jian Gon.
25 ***Multi-modal Fault-tolerant Control for single-phase cascade off-gird PV-storage system with PV failure using hybrid modulation***

Room C

Session cF2-2 - Wide bandgap power Devices: GaN and Ga2O3 device level reliability

Chairs: M. Meneghini, L. Theolier

09:00 **Andrea Natale Tallarico,** Niels Posthuma, Benoit Bakeroot, Stefaan Decoutere, Enrico Sangiorgi and Claudio Fiegna
105 ***Role of the AlGaN barrier on the long-term gate reliability of power HEMTs with p-GaN gate***

09:20 **Alessandro Borghese,** Michele Riccio, Giorgia Longobardi, Luca Maresca, Giovanni Breglio and Andrea Irace
109 ***Gate leakage current sensing for in situ temperature monitoring of p-GaN gate HEMTs***

09:40 **Arianna Nardo**, Meneghini, Barbato, De Santi, Meneghesso, Zanoni, Sicre, Sayadi, Prechtl and Curatola
145 ***Non thermally-activated transients and buffer traps in gan transistors with p-type gate: a new method for extracting the activation energy***

10:00 **Eleonora Canato,** Matteo Meneghini, Carlo De Santi, Fabrizio Masin, Arno Stockman, Peter Moens, Enrico Zanoni and Gaudenzio Meneghesso
204 ***OFF-state trapping phenomena in GaN HEMTs: Interplay between gate trapping, acceptor ionization and positive charge redistribution***

Invited talk

10:20 **Kornelius Tetzner**
INV3 ***Challenges to overcome breakdown limitations in lateral β-Ga2O3 MOSFET Devices***

10:50 Break

Stage (Room for All)

Industrial 2 - Hitachi Power Solutions Co., Ltd.

11:10 **Natsuki Sugaya**
IND2 ***High Throughput Ultrasonic Inspection Apparatus Using Quasi-static Water Surface Contact***

Room A

Session A3 – Quality and reliability assessment techniques and methods for devices and systems

Chairs: N. Stojadinovic, E. Olthof

11:30 **Ui-Min Choi,** Ionut Vernica, Dao Zhou and Frede Blaabjerg
72 ***Comparative evaluation of mission profile based reliability assessment methods of power modules in motor drive inverter***

11:50 Bahar Ahmadi, Richard Heredia, **Sina Shahbazmohamadi** and Zahra Shahbazi
234 ***Non-destructive automatic die-level defect detection of counterfeit microelectronics using machine vision***

12:10 **David Guillon,** Barbara Scherrer and Franc Dugal
68 ***Reliability test for subsea power semiconductors***

12:30 **Dawei Zhao,** Sebastian Letz, Zechun Yu, Andreas Schletz and Martin März
83 ***Combined experimental and numerical approach for investigating the mechanical degradation of the interface between thin film metallization and Si-Substrate after temperature cycling test***

Room B

Session bK-1 – Radiation impact on circuits and systems reliability

Chairs: F. Iannuzzo

11:30 **Marco Pocaterra** and Mauro Ciappa
240 ***Experimental setup to monitor non-destructive single ionization events caused in power devices by terrestrial cosmic radiation***

11:50 P. Balasubramanian, Douglas Maskell and **Nikos Mastorakis**
118 ***Asynchronous early output majority voter and a relative-timed asynchronous TMR implementation***

12:10 Giovanni Busatto, Antonio Di Pasquale, Daniele Marciano, Simone Palazzo, Annunziata Sanseverino and **Francesco Velardi**
265 ***Physical mechanisms for gate damages induced by heavy ions in SiC power MOSFET***

12:30 Marcio Goncalves, **Josie Esteban Rodriguez Condia,** Matteo Sonza Reorda, Luca Sterpone and Jose Rodrigo Azambuja
232 ***Improving GPU register file reliability with a comprehensive ISA extension***

Room C

Session cG2 – MEMS

Chairs: Massimo Vanzi, Loukas Michalas

11:30 **Maxime Auchlin,** Ivan Marozau, Dara Zaman Bayat, Laurent Marchand, Volker Gass, Olha Sereda

193 ***Can automotive MEMS be reliably used in space applications? An assessment method under sequential bi-parameter testing***

11:50 **Alexandra Koumela,** Loïc Joët, Audrey Berthelot, Patrice Rey and P. Brunet-Manquat

11 ***Robustness of a M&NEMS Pressure Sensor up to 522°C***

12:10 **Matroni Koutsoureli,** Dimitrios Birmpiliotis and George Papaioannou

133 ***A study of material stoichiometry on charging properties of SiNx films for potential application in RF MEMS capacitive switches***

12:30 **John Theocharis,** Matroni Koutsoureli, Spiros Gardelis, George Konstantinidis and George Papaioannou

77 ***Field emission induced-damage in the actuation paths of MEMS capacitive structures***

12:50 Break

Stage (Room for All)

Industrial 3 - SECTOR TECHNOLOGIES SAS

13:20 **Antoine Reverdy**

IND3 ***ThermoFisher static optical fault isolation roadmap and lock- in thermography for automotive***

Industrial 4 - SmarAct GmbH

13:40 **Marc Heinemann**

IND4 ***Presentation of the new SMARPROBE LX nanoprober system***

Poster Room

14:00 -15:30 Poster Session 3

3a: B - Failure mechanisms and reliability of micro- and nanoelectronics

34 **Martin Versen** and Wolfgang Ernst

Row hammer avoidance analysis of DDR3 SDRAM

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125 **Emmanuel Bender,** Joseph B. Bernstein and Alain Bensoussan

Reliability prediction of FinFET FPGAs by MTOL

---

218 **Jordan Locati,** Vincenzo Della Marca, Christian Rivero, Pascal Fornara, Arnaud Regnier, Stephan Niel and Karine Coulié

AC stress reliability study on a novel vertical MOS transistor for non-volatile memory technology

3b: C - Progress in failure analysis: defect detection and analysis

59 **Gwang Wook Lee,** Sunnu Shim, Wookhyun Cho, Wonse Kim, Kisoo Lee, Jaehyun Kim, Seongjun Cho, Seokjun Won and Bonyoung Koo
Novel failure traces beyond the Barrier on the floating device

---

78 Jae-Yeon Kim, **Jang-Hun Jo,** Jai-Won Byeon
Ultrasonic monitoring performance degradation of lithium ion battery

---

184 **Byongjin Ma**
Failure-analysis method of soldering interfaces in light-emitting diode packages based on time-domain transient thermal response

---

242 **Nicholas May,** Joseph Favata, Bahar Ahmadi, Pouya Tavousi and Sina Shahbazmohamadi
Correlative microscopy workflow for precise targeted failure analysis of multi-layer ceramic capacitors

3c: E - Packaging and assembly reliability and failure analysis

3 **Zhengwei Fan,** Xun Chen, Yao Liu, Yu Jiang and Yunan Zhang
Effects of anisotropy on the reliability of TSV microstructure

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61 **Motoki Eto,** Noritoshi Araki, Takashi Yamada, Robert Klengel, Sandy Klengel, Masaaki Sugiyama and Shinji Fujimoto
Reliability improvement for palladium coated copper wire using additive element

---

119 **Said Bensebaa,** Mounira Berkani, Stephane Lefebvre and Mickael Petit.
Reliability study of PCB-embedded power dies using solderless pressed metal foam

---

120 **Mohamad Nazar,** Ali Ibrahim, Zoubir Khatir, Nicolas Degrenne and Zeina Al-Masry
Remaining useful lifetime estimation for electronic power modules using an analytical degradation model

---

147 Chihiro Kawahara, **Julio Brandelero,** Stefan Mollov and Pierre-Yves Pichon
Effects of solder degradation on the die temperature measurement via internal gate resistance

---

157 **Bernhard Czerny** and Golta Khatibi
Interface characterization of Cu-Cu ball bonds by a fast shear fatigue method

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163 **Ali Ibrahim,** Zoubir Khatir, Jean-Pierre Ousten, Richard Lallemand, Nicolas Degrenne, Stefan Mollov and Damien Ingrosso
Using of bond-wire resistance as ageing indicator of semiconductor power modules

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169 Chang-Chun Lee**,** Kuo-Shu Kuo, **Chi-Wei Wang,** Jing-Yao Chang, Wei-Kuo Han and Tao-Chih Chang
Packaging reliability estimation of high-power device modules by utilizing silver sintering technology

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187 **Felix Wuest,** Olaf Wittler and Martin Schneider-Ramelow
Influence of temperature and humidity on power cycling capability of power modules

3d: G - Optoelectronics, Micro-Electro-Mechanical actuators and MEMS

196 **Jae-Seong Jeong**
Barrier properties analysis of Cu/TiW/ITO electrode for Si heterojunction solar cell under thermal aging

3e: H - ESD, EOS, Latch-up, EMC-EMI in integrated and power circuits

126 **Kraiem Sana,** Hamouda Mahmoud and Ben Hadj Slama Jalel
Conducted EMI mitigation in transformerless PV inverters based on intrinsic MOSFET parameters

---

156 **Philippe Galy,** Frederic Soto, Johan Bourgeat, Blaise Jacquier, Valeria Kilchytska and Denis Flandre
Experimental results on gated diodes and BIMOS ESD devices in 28nm FD-SOI under TLP & TID radiation

---

198 **Fabian Vargas,** Juliano Benfica, Matheus Fay Soares and Dorian Schramm
Conducted EMI susceptibility analysis of a COTS processor as function of aging

3f: L - Batteries, capacitors & passives

54 Diyin Tang, **Mengtong Gong,** Jinsong Yu and Xiang Li
A power transfer model-based method for lithium-ion battery discharge time prediction of electric rotatory-wing UAV

---

71 Puyu Wang, **Tao Yuan,** Qingwen Mou, Wei Gu, Zhengrong Xiang and Zhao Liu
Reliability analysis of excitation control modes of a synchronous condenser during grid-integration at the speed-falling stage

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173 Nicola Delmonte, David Cabezuelo, Iñigo Kortabarria, Danilo Santoro, Andrea Toscani and **Paolo Cova**
A method to extract lumped thermal networks of capacitors for reliability oriented design

---

210 **Jae-Yeon Kim,** Jin-Yeong Kim, Mu-Kyeong Kim and Jai-Won Byeon
Health monitoring of mechanically fatigued flexible lithium ion battery by electrochemical impedance spectroscopy

Thursday, October 8

Room A

Session aK2 - Radiation impact on circuits and systems reliability

Chairs: N. Melanitis

09:00 **Ze He,** Chang Cai, Tianqi Liu, Bing Ye, Lihua Mo and Jie Liu.
143 ***Heavy Ion and proton induced single event upsets in 3D SRAM***

09:20 **Gangping Yan,** Gaobo Xu, Jinshun Bi, Guoliang Tian, Huaxiang Yin, Yongliang Li and Qiuxia Xu
49 ***Accumulative total ionizing dose (TID) and transient dose rate (TDR) effects on planar and vertical ferroelectric tunneling-field-effect-transistors (TFET)***

09:40 **Tianqi Liu,** Dongqing Li, Chang Cai, Peixiong Zhao, Chen Shen, Jie Liu and Guangwen Yang
127 ***Heavy ion track straggling effect in single event effect numerical simulation of 3D stacked devices***

10:00 **Junchao Chen**, Thomas Lange, Marko Andjelkovic, Aleksandar Simevski and Milos Krstic
24 ***Prediction of solar particle events with SRAM-based soft error rate monitor and supervised machine learning***

Room C

Session H - ESD, EOS, Latch-up, EMC-EMI in integrated and power circuits

Chairs: G. Papaioannou

09:20 Wentao Qin, Dorai Iyer, Jim Steinwall, Robert Watkins, **George Chang,** Carroll Casteel, Jim Morgan and Mike Thomason
60 ***Microstructure evolutions upon Ni(Pt) silicidation and the different responses to the metal etch***

09:40 **Zhian Wang,** Binhong Li, Jianfei Wu, Wenxin Zhao, Bo Li, Hainan Liu, Chongjie Guan, Shiwei Feng, Jiajun Luo and Tianchun Ye
209 ***A comparison study on electromagnetic susceptibility of current reference circuits with scaling-down technologies and schemes***

10:00 **Laurine Curos,** Tristan Dubois, Guillaume Mejecaze, Frédéric Puybaret, Bernard Plano and Jean-Michel Vinassa
128 ***Investigation of critical parameters in power supplies components failure due to electric pulse***

Stage (Room for All)

Industrial 5 - John P. Kummer GmbH

10:20 **Jim Colvinn,** Tim Hazeldine
IND5 ***Improved Workflows in Topside and Backside Mechanical Sample Preparation***

10:40 Break

Room A

Session aF2-3 - Power electronic auxiliary circuits and system reliability

Chairs: M. Meneghini

11:00 **Massimo Vanzi** and Giovanna Mura
80 *Peculiar failure mechanisms in GaN power transistors*

11:20 **Maria Ruzzarin,** Karen Geens, Matteo Borga, Hu Liang, Shuzhen You, Benoit Bakeroot, Stefaan Decoutere, Carlo De Santi, Andrea Neviani, Matteo Meneghini, Gaudenzio Meneghesso and Enrico Zanoni
195 *Exploration of gate trench module for vertical GaN devices*

11:40 **Nicola Modolo,** Matteo Meneghini, Alessandro Barbato, Arianna Nardo, Carlo De Santi, Gaudenzio Meneghesso, Enrico Zanoni, Sebastien Sicre, Gerhard Prechtl and Gilberto Curatola
148 *A Novel on-wafer approach to test the stability of GaN-based devices in hard switching conditions: study of hot-electron effects*

12:00 **Maximilian Goller,** Marc André Thim, Jianhua Song, Jens Kowalsky, Jörg Franke and Josef Lutz.
226 *Investigation of the Current Collapse behaviour in GaN Power HEMTs with highly adjustable pulse and measurement concept*

Invited talk

12:20 **Martin Kuball**
INV4 *Gallium Nitride on Diamond*

Room B

Session bL - Batteries, capacitors and passives

Chairs: Spiros Gardelis

11:00 Xinpeng Qu, Datong Liu, **Yuchen Song,** Xiuhai Cui and Yu Peng.
95 *Lithium-ion Battery Performance Degradation Evaluation in Dynamic Operating Conditions based on a Digital Twin Model*

11:20 **Matthieu Maures,** Armande Capitaine, Jean-Yves Delétage, Jean-Michel Vinassa, Olivier Briat
192 *Lithium-ion battery SoH estimation based on incremental capacity peak tracking at several current levels for online application*

11:40 **Hao Niu**, Shujuan Wang and Xuerong Ye
168 *Reliability-oriented optimization of aluminum electrolytic capacitor considering uncertain mission profile*

12:00 **Chunlin Lv,** Jinjun Liu, Yan Zhang, Wanjun Lei and Rui Cao
74 *An improved lifetime prediction method for metallized film capacitor considering harmonics and degradation process*

Room C

Session cG2 – MEMS

Chairs: M. Vanzi, L. Michalas

11:00 Pierre Janioud, **Christophe Poulain,** Alexandra Koumela, Jean Marc Armani, Antoine Dupret, Patrice Rey, Audrey Berthelot, Guillaume Jourdan and Panagiota Morfouli.
84 ***Effects of gamma radiation on suspended silicon nanogauges bridge used for MEMS transduction***

11:20 **Antoine Nowodzinski**
75 ***Capacitive micromachined ultrasonic transducers leak detection by dye penetrant test***

11:40 **Dimitrios Birmpiliotis,** Matroni Koutsoureli, George Stavrinidis, George Konstantinidis and George Papaioannou
76 ***A study of hopping transport during discharging in SiNx films for MEMS capacitive switches***

12:50 Break

Stage (Room for All)

13:10 Session INV: Invited - Best Paper Awards

Stage (Room for All)

14:10 ESREF 2020 - Closing Remarks

Chair: George Papaioannou

Abstracts

T1 *III-Nitrides Substrates and Defect Characterization in Nitride Materials for Power Devices*

Elke Meissner (Fraunhofer IISB, Erlangen).

Abstract

The performance and reliability of an electrical device is decisive for its application and wider usage. Novel devices often show an outstanding performance in laboratory environment but have to survive field conditions and perform free of failure for a long time. If a failure of the device occurs, the origin has to be identified and may have various causes ranging from materials defects over processing issues, packaging problems and others. This tutorial will pick up this topic from a materials point of view and will discuss what defects in the materials are considered relevant for the electrical function of a nitride device and how such materials defects can be analyzed. Thereby, materials issues in the substrates starting from crystal growth of GaN and AlN will be discussed as well as defects in epitaxial layers for device structures. The tutorial points out a possible methodology how to identify key defects in nitride materials with respect to the performance of a power device.

T2 *Vertical GaN devices and reliability*

Tetsu Kachi (Nagoya University Japan, Toyoda Central Research Laboratory).

Abstract

The vertical structure of the power device has advantages such as small chip size, easy wiring, and high breakdown voltage. Furthermore, wideband gap semiconductors have the greatest feature of low on-resistance. GaN is a material having the ability to fully exhibit these properties and in recent years development of GaN vertical devices has been accelerated. For example, GaN vertical devices with over 1kV breakdown voltage have been reported recently. Moreover, over 3kV pn diodes were also reported. Therefore, ability of GaN for high voltage devices has already been proven. Next issues are developments of fabrication process technologies which make devices stable operation. In this presentation, we will report recent our advances in process technologies for GaN vertical devices, which are high quality GaN epitaxial growth technology, dry etching technology for trench forming of MOSFET, and Mg ion implantation and its activation for p-GaN. Especially, the Mg ion implantation will make it possible to expand the freedom of the device design and simplify the device process. return

KN1 *Reliability in the era of electrification in aviation: a systems approach*

Konstantinos Emmanouil (Rolls-Royce Deutschland).

Abstract

With an increasing amount of electrification projects in aviation, reliability becomes a key question. Integrating electric and electronic equipment in areas that have been dominated by thermal machines poses big challenges and opportunities. This presentation will provide insights into the methods used to determine the required reliability by assessing the whole system and exploring the electromechanical and environmental interactions that define the new requirements to be met. Finally, it will discuss the interlinked nature between safety and reliability in aviation. return

KN2 *Title –High-resolution non-destructive three-dimensional imaging of integrated circuits*

Gabriel Aeppli (Department of Physics, ETH Zürich, Switzerland Institut de Physique, EPFL, Switzerland Paul Scherrer Institut).

Abstract

It is remarkable that semiconductor technology is more advanced in its capacity to create complex systems than in the ability to image the outcomes. Conventional high-resolution microscopy for imaging the interior of three-dimensionally structured objects typically entails destructive sample preparation followed by electron microscopy of resulting surfaces or sections. Here we describe X-ray ptychography, a mixed real space/reciprocal space („wavelet“) technique, which is non-destructive and provides three-dimensional images at steadily improving resolution, which have now reached 15 nanometers. We show applications to integrated circuit inspection, and describe implications for security and quality control.

KN3 *Reliability Limitations from Crystal Defects in Thick GaN Epitaxial Layers for Power Electronics*

Aris Christou (University of Maryland, Dept. of Materials Science and Engineering and Mechanical Engineering Department).

Abstract

The state-of-the-art power switching devices made from GaN semiconductors contain a high density of crystal defects, especially in the thick epitaxial layers. Most of these defects are present initially in starting wafers and some are generated during device processing. There is little conclusive evidence so far on the exact role that the crystal defects play on device performance, manufacturing yield, and more importantly, long-term field-reliability especially when devices are operating under extreme stressful high voltage environments. This paper provides the progress of characterization of thick GaN power semiconductor material epitaxial layers and growth technology, and the potential impact crystal defects may have on high-density power switching electronics. A comparison of the SiC development and manufacturing evolution is made to draw a parallel between SiC and GaN wide bandgap (WBG) semiconductor power electronics. return

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INV1 Fail-to-open short-circuit failure mode in SiC power MOSFETs, device characterization and system level exploitaton

Alberto Caztellazzi (Kyoto University of Advanced Science).

Abstract

"A class of SiC power MOSFETs have recently been found to feature a fail-to-open failure mode, with the device going into permanent automatic shut-down mode. Such behavior is extremely interesting for the application. In the frequent case of power converters designed with parallel connected devices or multi-chip power modules, a fail-to-open implies loss of a single device, but does not compromise the possibility to still operate the system, even if at reduced power levels (hopping home modality). More recently, it has also been shown that in the case of progressive moderate damage accumulation, the degradation of the device characteristics can be recovered to a stable state by ad-hoc biasing of the device itself. This talk will review the degradation and failure mechanisms leading to fail-to-open signature, will present evidence of stable device recovery capability and present ideas and solutions to make use of such feature in the application. The results are substantiated by extensive functional and structural device characterization" *return*

INV2 *3D and compact thermal modeling in power electronics: an overview*

Nicola Delmonte (Department of Engineering and Architecture, University of Parma).

Abstract

Thermal management is a key point of power converters development because it affects their performance defining heat flow and temperature cycling. Even if cooling technologies for electronics have been a

research topic since the birth of power electronics, in the last decade the number of publications related to this field has grown significantly. This is because thermal management, with the power density increasing and the high reliability required by many applications, cannot be the same of old systems. Then, here it will be presented an overview of cooling techniques for power electronics and the numerical modeling related to thermal management problems. It will be shown different numerical analysis based on multiphysics Finite Element Analysis and compact thermal models, such as the Foster and Cauer networks, which can be useful for SPICE-like electro-thermal simulations. The aim is to show how multiphysics simulations can be used for the cooling system design or for reliability studies.

INV3 *Challenges to Overcome Breakdown Limitations in lateral β-Ga2O3 MOSFET Devices*

Kornelius Tetzner (Ferdinand-Braun-Institut, Berlin FBH, Germany).

Abstract

Due to the large band gap of 4.8 eV and the resulting high breakdown strength of 8 MV/cm, the semiconductor material β-Ga2O3 has a very promising potential for next-generation power electronic applications. The higher breakdown strength compared to established technologies based on SiC or GaN allows a much more compact design of the transistor structures, which leads to reduced switching and conduction losses. This enables far more efficient, lighter and smaller power electronic converters to be implemented than it is possible today. In this talk the fabrication of high-performance metal-oxide-semiconductor field-effect transistors (MOSFETs) on Si-doped homoepitaxial layers on (100) Mg-doped semi-insulating β-Ga2O3 substrates is presented. The fabricated devices exhibit maximum drain currents, on/off-current ratios and ON-resistances of ~75 mA/mm,109 and 110 Ω·mm, respectively. Moreover, breakdown voltages at around 1200 V for devices with a gate-to-drain distance of 6 µ m are measured which equals an average breakdown field strength of 2 MV/cm. Further investigations on devices with and without field-plates reveal interface-related material inconsistencies which might represent the current main limitation factor in reaching high breakdown voltages in β-Ga2O3 MOSFET devices. *return*

INV4 *Gallium Nitride on Diamond*

Martin Kuball (School of Physics, Bristol University, UK).

Abstract

Gallium Nitride (GaN) electronics is transforming what communication and radar system can deliver, and are presently mostly based on GaN-on-SiC technology; though SiC is a material of good thermal conductivity (450 W/mK) the devices are still thermally limited which restricts the power density achievable with GaN technology. Diamond substrates which can have more than six times greater thermal conductivity than SiC provide a pathway to overcome the thermal limitations of GaN-on-SiC technology. However integrating both GaN and diamond has its challenges including due to the coefficient of thermal expansion mismatch of both materials. The latest developments in this field will be presented, including different integration approaches to maximize thermal heat extraction from the active device region to device results.

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3 *Effects of anisotropy on the reliability of TSV microstructure*

Zhengwei Fan (National University of Defense Technology), Xun Chen (National University of Defense Technology), Yao Liu (National University of Defense Technology), Yu Jiang (National University of Defense Technology) and Yunan Zhang (National University of Defense Technology).

Abstract

This article explored in detail the influence of the anisotropy of silicon and copper on the reliability of TSVs, and particularly focused on the coupled effect of anisotropic of silicon and copper. In addition, the influence of copper plasticity was also analyzed. The results show that a strong anisotropy will significantly increase

the crack propagation capability at the structural interface and threaten device reliability. And the anisotropic coupling effect of copper and silicon will further amplify the impact. Besides, the plasticity of TSV-Cu cannot be ignored in the analysis of the reliability of the TSV structure as it has a significant effect on the crack growth. *return*

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4 *PV system performance and failure evaluation of 10 year field-aged 1-MW PV power plant*

Wonwook Oh (STECO corporation), Hoonjoo Choi (STECO), Kun Won Seo (STECO), Haeseok Lee (Korea University), Donghwan Kim (Korea University), Daesung Kim (STECO corporation), So-Yeon Kim (Republic of Korea Naval Academy) and Heon Hwang (Sung Kyun Kwan University).

Abstract

Photovoltaic (PV) power systems have been rapidly installed worldwide in recent years. It is believed that PV power plants will operate stably for more than 25 years. However, PV modules can fail unexpectedly. In this paper, we have diagnosed a 10-year-old power plant using a drone with an infra-red (IR) camera and recorded current-voltage (I-V) and electroluminescence (EL) measurements. The ~1-MW plant, comprising two different PV modules—of 200 and 220 W—showed various failure modes, and approximately 59% of PV module failures caused an output loss. An inverter with a serious loss is expected to degrade to an extent exceeding its annual degradation rate in PV strings above 40%. As a result, the power loss was quantitatively estimated considering hotspots, bypass diode failure, and the degradation rate. The capacity of the current PV system was evaluated to be 88.3% and 93.2% for the two types of PV modules. *return*

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8 *Modeling and analysis of the catastrophic failure and degradation data*

Seung Hyun Kim (Samsung Electronics) and Si-Il Sung (Kyonggi University).

Abstract

In this paper, we are concerned with the reliability models and analysis methods for the case where catastrophic and degradation failure modes are considered simultaneously. First, the existing degradation models and analysis methods are reviewed and classified. In particular, the existing methods for analyzing degradation data are classified into the “horizontal axis” and “vertical axis” methods. Second, based on the above degradation models and analysis methods, a systematic procedure for simultaneously analyzing catastrophic failure times and degradation measurement data are presented. Finally, using the data in Huang and Askin [1], comparative analysis results are presented with respect to the direction of analysis (i.e., horizontal versus vertical). return

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9 *Effect of the cell size reduction on the threshold voltage of UMOSFETs*

Yoshiro Baba (Kyusyu Institute of Technology) and Ichiro Omura (Kyushu Institute of Technology).

Abstract

UMOSFET on-resistances have been dramatically improved in recent decades with the miniaturization of cell size by innovations in the fabrication process. However, with miniaturization, failure in the gate oxide, large deviations in the threshold voltage and reductions in avalanche capability have emerged as design problems for mass production. In particular, rises in the gate threshold voltage can cause significant damage to the yield in MOSFET mass production. Threshold voltage rises have appeared with the introduction of a trench source contact. The source contact trench and MOS gate trench are fabricated next to each other with a narrow silicon mesa region, and the voltage rises appear when the silicon mesa width becomes narrower than 80 nm. So far, it appears that the P+ layer dopant in the contact sidewall diffuses toward the gate oxide and the channel doping increases, which causes the rise in the threshold voltage Vth. We analyzed the distribution of Vth at the wafer level/shot level and found for the first time that the rise in Vth is caused by the punch-through effect from the channel depletion layer to the contact P+ layer, and thus, sidewall dopant diffusion will not affect the rise in Vth. We established an analytical model for the rise in Vth and validated the model by comparing it with UMOSFET production data. Our model showed that for

the field plate type UMOSFET with a shorter gate contact length, not only is there a rise in Vth, but also it is difficult to control Vth using the conventional channel implantation method. *return*

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11 *Robustness of a M&NEMS Pressure Sensor up to 522°C*

Alexandra Koumela (CEA-LETI), Loïc Joët (CEA-LETI), Audrey Berthelot (CEA-LETI), Patrice Rey (CEA-LETI) and P. Brunet-Manquat (CEA-LETI).

Abstract

This paper examines the reliability of pressure sensors fabricated with the M&NEMS technology up to 522°C. The results are quite promising as we observe only a small decrease (6%) of the sensor sensitivity after thermal cycling. The packaging of the sensor seems to well withstand these temperatures and the only limit that is identified is the metallization of the pads which could be improved in order to have functional devices at higher temperatures. *return*

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12 *Impact of Sensing Current Density on PN-Junction Based Temperature Estimation Methods for Si and SiC Power Devices*

Felix Hoffmann (University of Bremen), Sarah Rugen (University of Bremen), Dieter Silber (University of Bremen) and Nando Kaminski (University of Bremen).

Abstract

In this work the impact of the sensing current density on the virtual junction temperature estimation methods for Si IGBTs and SiC MOSFETs using the pn junction voltage drop as TSEP was investigated. For this purpose, measurements of the temperature characteristics at different sensing current densities were performed on several Si and SiC devices. Additionally, TCAD simulations were performed to verify the measurement results. So far, 0.1% of the devices nominal current is commonly accepted as guideline for sensing currents for Si IGBTs and with the results of this investigation, this guideline was verified and examined towards their applicability for SiC MOSFETs. The results indicate that the 0.1% of the devices nominal current yield an applicable sensing current for Si IGBTs but is not applicable for SiC MOSFETs. *return*

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14 *Modeling and Fault Diagnosis of Multi-phase Winding Inter-turn Short Circuit for Five-phase PMSM based on Improved Trust Region*

Jianwei Yang (Xi'an University of Posts and Telecommunications), Zhiyong Dai (Xidian University) and Zhen Zhang (Chang'an University).

Abstract

Multi-phase PMSMs are widely used in fault-tolerant control applications. As an electrical fault with a high probability, inter-turn short circuit (ITSC) fault seriously affects the reliability of five-phase PMSM. However, due to high coupling of fault parameters, most of the fault models and diagnosis methods in fault-tolerant control focus on one-phase winding ITSC fault of three-phase PMSM. In this paper, a novel model and a fault diagnosis method are proposed for multi-phase winding ITSC (MPWITSC) of five-phase PMSM. First, by analyzing the related physical parameters of the motor, a mathematic model of MPWITSC fault is established. Then, a parameter estimation method based on improved trust region (ITR), which accelerates the convergence speed of traditional trust region (TTR) and reformulates the fault diagnosis as the extreme seeking for fault parameters is proposed to detect the ITSC fault level. Experimental results provide verification of the proposed model and fault diagnosis method. *return*

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15 *A reliability evaluation method for multi-performance degradation products based on the Wiener process and Copula function*

Guangze Pan (China Electronic Product Reliability and Environmental Testing Research Institute), Yaqiu Li (China Electronic Product Reliability and Environmental Testing Research Institute), Xiaobing Li (China Electronic Product Reliability and Environmental Testing Research Institute), Qin Luo (China Electronic Product Reliability and Environmental Testing Research Institute), Chunhui Wang (China Electronic Product Reliability and Environmental Testing Research Institute) and Xianghong Hu (China Electronic Product Reliability and Environmental Testing Research Institute).

Abstract

This paper is intended to propose a reliability evaluation method for products with high-reliability, long-life, small samples and multi-performance degradation. The Wiener process is used to model the degradation of a single performance parameter of the product to obtain its reliability evaluation model, since this can effectively describe the randomness of the product performance degradation process. Afterward, the Copula function is used to model the degradation of multiple performance parameters of the product, and a comprehensive determination method of the Copula function is proposed which can more accurately and effectively describe the coupled competition relationship of multi-performance degradation. Finally, the reliability evaluation of an insulated gate bipolar transistor is carried out, and the evaluation results are compared with the evaluation results of a single performance parameter, multiple independent performance parameters, and the actual case. The results show that the method proposed is more accurate and more applicable than traditional methods. *return*

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17 *Profiling of carriers in a 3D flash memory cell with nanometer-level resolution using scanning nonlinear dielectric microscopy*

Jun Hirota (Kioxia Corp.), Kohei Yamasue (Tohoku univeristy) and Yasuo Cho (Tohoku University).

Abstract

Carrier distributions in the floating gate and channel structures with sizes <10 [nm] of 3D Flash memory cells were clearly measured by using scanning nonlinear dielectric microscopy (SNDM). Using super-sharp diamond tips with radius of <5 nm to achieve the supreme spatial resolution, we successfully obtained SNDM signals of floating gate in high contrast to the background. We deduced the minimum spatial resolution and confirmed that our SNDM exhibits the spatial resolution as good as < 1.9 [nm]. Furthermore, we seized a clear evidence that the diffusion length differences of the n-type impurity among the channels are < 21 [nm]. These mean that we successfully established an exceptionally effective method for the device performance optimization and the device failure analysis. *return*

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18 *Spatial scale dependent impact of non-uniform interface defect distribution on field effect mobility in SiC MOSFETs*

Kohei Yamasue (Tohoku university) and Yasuo Cho (Tohoku University).

Abstract

We discuss the impact of the non-uniformity in interface defect distribution at a SiO2/SiC interface on the field effect mobility of SiC metal oxide semiconductor field effect transistors. By device simulation based on interface defect distribution experimentally observed by local deep level transient spectroscopy, we show that interface defect distribution containing smaller features gives higher impact on the field effect mobility. *return*

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22 *Fault diagnosis of cracks in crystalline silicon photovoltaic modules through I-V curve*

Mingyao Ma (Hefei University of Technology), Zhixiang Zhang (Hefei University of Technology), Heng Liu (Hefei University of Technology), Ping Yun (Sungrow Power Supply Co., Ltd.), Xing Zhang (Hefei University of Technology) and Fei Li (Hefei University of Technology).

Abstract

This paper focuses on the crack problem of silicon photovoltaic（PV） modules. In order to extract the fault characteristics of the cracked PV modules, we investigate and collect the cracked PV modules in several large PV power plants. The I-V characteristics of the cracked PV modules are tested. The test results show that the I-V curves of the cracked PV modules show a convex function step, and the reason for the I-V characteristics of the cracked PV module is analysed. A method for online diagnosis of PV module crack through I-V curve is proposed. *return*

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23 *Online Junction Temperature Estimation Using Integrated NTC Thermistor in IGBT Modules for PMSM Drives*

Mingyao Ma (Hefei University of Technology), Xuesong Yan (Hefei University of Technology), Weisheng Guo (Hefei University of Technology), Shuying Yang (Hefei University of Technology), Guoqing Cai (Sungrow Power Supply Co., Ltd.) and Wenjie Chen (Sungrow Power Supply Co., Ltd.).

Abstract

Junction temperature fluctuations of power modules in electric vehicles (EV) have a significant impact on system reliability. This paper aims to estimate the junction temperature of IGBT modules with direct coolant for permanent magnet synchronous motors (PMSM) under complex boundary conditions. The advantage of the thermal network proposed in this article is that it does not require any temperature sensor except the built-in negative thermal coefficient (NTC) thermistor. Finally, the good accuracy of this model is demonstrated by a series of experiments considering complicated boundary conditions and multiple working conditions. *return*

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24 *Prediction of Solar Particle Events with SRAM-Based Soft Error Rate Monitor and Supervised Machine Learning*

Junchao Chen (Innovations for High Performance Microelectronics), Thomas Lange (iRoc Technologies; Dipartimento di Informatica e Automatica, Politecnico di Torino), Marko Andjelkovic (Innovations for High Performance Microelectronics), Aleksandar Simevski (Innovations for High Performance Microelectronics) and Milos Krstic (Innovations for High Performance Microelectronics; University of Potsdam).

Abstract

This paper introduces an embedded approach for the prediction of Solar Particle Events (SPEs) by combining the real-time Soft Error Rate (SER) measurement with SRAM-based detector and the supervised machine learning model. The proposed approach is intended for the self-adaptive fault tolerant multiprocessing systems employed in space applications. With respect to the state-of-the-art, our solution brings three benefits: (1) early prediction of SPE occurrence at least one hour in advance, (2) fine-grained hourly tracking of SER variations during SPEs and under normal conditions, and (3) tight integration in the existing hardware, reducing the necessary overhead to minimum. Based on comparison of five different machine learning algorithms trained with the public space flux database, the preliminary results indicate that the best prediction accuracy is achieved with the recurrent neural network (RNN) with long short-term memory (LSTM). *return*

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25 *Multi-modal Fault-tolerant Control for Single-phase Cascade Off-gird PV-storage System with PV Failure Using Hybrid Modulation*

Yiyan Lu (School of Automation, Nanjing University of Science and Technology, Nanjing, China), Zhao Liu (School of Automation, Nanjing University of Science and Technology, Nanjing, China), Jianshou Kong (School of Automation, Nanjing University of Science and Technology, Nanjing, China) and Jian Gong (School of Automation, Nanjing University of Science and Technology, Nanjing, China).

Abstract

An optimized fault-tolerant control for single-phase cascade off-grid photovoltaic(PV)-storage system with PV failure is proposed in this paper. Depending on states of PVs, the proposed fault-tolerant control utilizes

operating modes analysis to enhance reliability of the system. The operating modes of normal running, partial PV failure, and full PV failure are analysed and control strategies for each mode is proposed respectively. Hybrid modulation is employed in all modes to reduce switching losses. The feasibility and effectiveness of the proposed control is validated by simulation results. The experiment results will be presented in the full paper. *return*

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27 *An active thermal management strategy for switched reluctance drive system with minimizing current sampling delay*

Qingqing Yang (Hefei University of Technology), Mingyao Ma (Hefei University of Technology), Shuying Yang (Hefei University of Technology) and Xing Zhang (Hefei University of Technology).

Abstract

Abstract – The reliability of switched reluctance drive system (SRD) can be improved by an effective thermal management strategy, when SRD is exposed to harsh environment and anything could happen throughout the life time. In order to avoid overtemperature fault of power converter, there are generally two methods: derating and switching frequency reduction. However, the derating methods will lead to insufficient power and even affect the safety of SRD. An active thermal management strategy for SRD with minimizing current sampling delay is proposed in this paper, which can ensure that the temperature of power converter will not exceed the maximum allowable temperature under any working condition by adjusting switching frequency. In the proposed strategy, the sampling method can ensure that the output performance of SRD at low switching frequency is not poorer than that of traditional sampling method at normal switching frequency by optimizing the sampling point. *return*

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28 *Optimal Sampling for Accelerated Testing in 14nm FinFET Ring Oscillators*

Shu-Han Hsu (Georgia Tech Institute of Technology), Ying-Yuan Huang (Georgia Tech Institute of Technology), Yi-da Wu (Georgia Tech Institute of Technology), Kexin Yang (Georgia Tech Institute of Technology), Li-Hsiang Lin (Georgia Tech Institute of Technology) and Linda Milor (Georgia Institute of Technology).

Abstract

The accuracy of accelerated lifetime tests may vary due to the choice of test conditions, which presents a problem in interpreting results. Furthermore, testing is generally performed on test structures which are simplified compared to circuits and systems. To better understand actual usage conditions, we use 14nm FinFET ring oscillator circuits instead as the test vehicle for accelerated testing, focused on detecting front-end time dependent dielectric breakdown. We investigate factors for minimizing errors in lifetime estimation, such as effects of sample size at various test points for different testing times and numbers of stages. *return*

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29 *Ageing of glass passivated TRIAC devices under thermal and electrical stress*

Yoann Buvat (STMicroelectronics, Tours, France / GREMAN UMR-CNRS 7347, Université de Tours, INSA Centre Val de Loire, Tours, France), Emilien Bouyssou (STMicroelectronics, Tours, France / GREMAN UMR-CNRS 7347, Université de Tours, INSA Centre Val de Loire, Tours, France), Benjamin Morillon (STMicroelectronics, Tours, France) and Gaël Gautier (GREMAN UMR-CNRS 7347, Université de Tours, INSA Centre Val de Loire, Tours, France).

Abstract

A new silicate glass passivation was studied on Metal-Dielectrics-Semiconductor structures to characterize the reliability performances of TRIAC devices. The presence of mobile ions was identified in the glass affecting the reliability performances. The addition of a semi-insulating passivation layer turns out to drastically improve the reliability performances of TRIAC devices. *return*

31 *Impact of electrical stress on total ionizing dose effects on graphene nano-disc non-volatile memory devices*

Kai Xi (Institute of Microelectronics Chinese Academy of Sciences) and Jinshun Bi (Institute of Microelectronics Chinese Academy of Sciences).

Abstract

The impact of electrical stress on the effects of total ionizing dose (TID) on graphene nano-disc non-volatile memory (GND-NVM) devices is investigated by X-ray irradiation with doses ranging from 50 to 1000 krad (Si). The electrical characteristics of the devices are measured at each dose step and are compared to those before X-ray exposure. Applying non-zero gate stress during irradiation significantly accelerates the degradation process, and the device fails with an unusable memory window at a TID dose of 500 krad (Si). The electric field in the surrounding oxides plays a key role in the observed degradation. *return*

32 *Study of temperature dependence of breakdown voltage and AC TDDB reliability for thick insulator film deposited by plasma process*

Tatsuya Ohguro (Toshiba Electronic Devices & Storage Corporation), Yuki Yagi (Toshiba Electronic Devices & Storage Corporation) and Yukiko Kashiura (Toshiba Electronic Devices & Storage Corporation).

Abstract

In this paper, temperature dependence of breakdown voltage (Vbd) and time-to-failure (TTF) in TDDB for thick insulator film (300nm) deposited by plasma process are discussed. In SiO2 film used TEOS and O2 gases, increase of both Vbd and TTF beyond 100 ℃ is reported for the first time. On the other hand, in the SiO2 film and SiN film involving nitrogen, both Vbd and TTF decrease with increasing temperature. In order to explain these difference, we focused on the type of conductivity and introduced de-trapped effect by thermal energy. In the film used TEOS and O2 based SiO2 gases, the temperature dependence of number of trapped carrier is smaller because the conductivity type is the FN tunnelling, while the number of de-trapped carrier significantly increases with temperature and the TTF beyond 100 ℃ becomes longer. In the film involving nitrogen, the de-trapped effect is negligible because the number of trapped carrier exponentially increases with temperature like Poole-Frenkel conductivity. *return*

34 *Row hammer avoidance analysis of DDR3 SDRAM*

Martin Versen (Technische Hochschule Rosenheim) and Wolfgang Ernst (Siemens AG).

Abstract

A DDR3 SDRAM test setup implemented on the Griffin III ATE test system from HILEVEL Technologies is used to analyse the row hammer bug. Row hammer pattern experiments are compared to standard retention tests for different manufacturing technologies. The row hammer effect is depending on the number of stress activation cycles. The analysis is extended to an avoidance scheme with refreshes similar to the Target Row Refresh scheme for the DDR4 SDRAM technology. *return*

36 *Mitigating single event upset of FPGA for the onboard bus control of satellite*

Xiuhai Cui (Harbin Institute of Technology) and Liansheng Liu (Harbin Institute of Technology).

Abstract

This paper proposes a hybrid anti-radiation method to enhance the reliability of Field Programmable Gate Array (FPGA), which is being applied more and more in the commercial small satellite. The method utilizes the advantages of Error Detection And Correction (EDAC) and Triple Modular Redundancy (TMR). Different bus control units are improved by different anti-radiation techniques. For finite state machine, dual-port block random access memory and EDAC are utilized. Hamming code is used to enhance First In First Output

unit. For the simple control register, TMR is applied to improve its anti-radiation. This hybrid method can avoid the accumulated error of TMR and reduce the complexity of system. Experimental results show that the proposed method can correct 1-bit error and detect 2-bit error effectively. *return*

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38 *Three-level inverters improve reliability based on equivalent input disturbance and repetitive control combinations*

Guoliang Yang (College of Electrical Engineering, Yanshan University,Qinhuangdao, Hebei 066004, China), Jinze Yin (College of Electrical Engineering, Yanshan University,Qinhuangdao, Hebei 066004, China), Zhiying Huang (The Bayin Guoleng Vocational and Technical College, korla, 841000, China) and Yuna Zhang (College of Electrical Engineering, Yanshan University,Qinhuangdao, Hebei 066004, China).

Abstract

In this paper, based on the harmonic problem appearing in the voltage, it is proposed to apply the repetitive control with equivalent input disturbance (EID) in the diode clamp type three-level inverter to obtain a smooth and stable output voltage waveform. The effectiveness of the control method is verified. The results show that this combined control method can effectively suppress the periodic and non-periodic disturbances in the system and improve the reliability of the whole system. *return*

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40 *Analysis Of Drain Current Transient Stability Of AlGaN/GaN HEMT stressed under HTOL & HTRB, By Random Telegraph Noise And Low Frequency Noise Characterizations*

Jean-Guy Tartarin (LAAS-CNRS and University of Toulouse), Oana Lazar (Thales Alenia Space), Alexandre Rumeau (LAAS-CNRS), Bernard Franc (LAAS-CNRS), Laurent Bary (LAAS-CNRS) and Benoit Lambert (UMS).

Abstract

The charges in wide bandgap Gallium Nitride (GaN) High Electron Mobility Transistors (HEMT) can be identified by means of various methods such as electrical transient, time or frequency domain pulsed characterization, or noise spectroscopy methods, usually performed at different temperatures to extract activation energies. These traps can be neutralized or activated with electrical or thermal conditions over a lifetime. Therefore, the distinction between harmful traps (with consequences on performances) and harmless traps (without impact on electrical behaviour) must be performed. In this paper, devices stressed by HTOL (High Temperature Operating Life) and HTRB (High Temperature Reverse Bias) are characterized by time domain electrical techniques (transient and pulsed), and with low frequency noise (LFN) tools. By performing characterizations on the gate and on the drain accesses, it is also possible to target the drain current sensitivity IDS to specific regions of the transistor. Many papers are available concerning the identification of traps, some offer cross-analyses of the defects, and develop a fine analysis of their correlation with the electrical behaviour of transistors before and after the application of a stress. The proposed case study tracks the traps or charges in the different zones of the transistor, and makes correlations with static or transient evolutions of IDS. *return*

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41 *Solving Time-dependent Reliability-based Design Optimization by Adaptive Differential Evolution Algorithm and Time-dependent Polynomial Chaos Expansions(ADE-T-PCE)*

Xuerong Ye (Harbin Institute of Technology), Hao Chen (Harbin Institute of Technology), Yue Wang (Harbin Institute of Technology), Hao Niu (Harbin Institute of Technology), Guofu Zhai (Harbin Institute of Technology), Wenwen Li (State grid jibei marketing service center(metrology center)) and Ruiming Yuan (State grid jibei marketing service center(metrology center)).

Abstract

Abstract – It remains a great challenge to investigate time-dependent reliability-based design optimization (TRBDO) problems, owing to the high computational cost of time-dependent reliability analysis, and the difficulties to model. To address these issues, ADE-T-PCE, a methodology incorporating an adaptive differential evolution (ADE) algorithm and an enhanced instantaneous time-dependent polynomial chaos expansions (T-PCE) is proposed. In the proposed method, the universal polynomial chaos expression (PCE) method was improved based on time-domain extension and principal component selection partial least squares, the life-cycle reliability model of time-dependent PCE is formed. Once the time-dependent model is built, time-dependent reliability can be computed conveniently. Consequently, dynamic niche Pareto optimal solution selection strategy, particle variations and and optimal solution screening strategy, number and strategy of particle variation for the differential evolution algorithm were proposed to meet demands for multi-object time-dependent reliability design optimization. The effectiveness of proposed method was verified by an electromagnetic relay in electric vehicles coupled with multiple degeneration factors in this study. *return*

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42 *Reliability-driven pin assingment optimization to improve in-orbit soft-error rate*

Ygor Q. Aguiar (Université de Montpellier - IES/RADIAC), Frédéric Wrobel (Université de Montpellier - IES/RADIAC), Jean-Luc Autran (Aix-Marseille Université), Paul Leroux (University of Leuven - KU Leuven), Frédéric Sagné (Université de Montpellier - IES/RADIAC), Vincent Pouget (Université de Montpellier - IES/RADIAC) and Antoine Touboul (Université de Montpellier - IES/RADIAC).

Abstract

This paper provides a pin assignment optimization in logic gates to improve in-orbit soft-error rate. Signal probability is used to assign the lowest probability to the most sensitive input combination of the circuit. An optimized cell netlist can achieve from 5% to 35% reduction on the in-orbit Single-Event Transient (SET) rate. *return*

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44 *Fretting wear reliability assessment methodology of gold-plated electrical connectors considering manufacture parameters distribution*

Sanqiang Ling (Harbin Institute of Technology), Le Xu (Harbin Institute of Technology), Donghui Li (Harbin Institute of Technology) and Guofu Zhai (Harbin Institute of Technology).

Abstract

Relatively little is known about the influence of manufacture parameters distribution on the reliability of electrical connectors under fretting conditions. In order to investigate the fretting wear lifetime of electrical connectors, an estimation model is proposed. The theoretical model of normal contact force for connector is established. Then, the initial model of electrical connectors is constructed utilizing the Monte Carlo sampling method and the distribution of normal contact forces is analyzed. In addition, the corresponding fretting wear lifetime is calculated based on the estimation model, and then its distribution type and distributing parameters are obtained. Finally, the reliability assessment method of electrical connectors is completed. *return*

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49 *Accumulative total ionizing dose (TID) and transient dose rate (TDR) effects on planar and vertical ferroelectric tunneling-field-effect-transistors (TFET)*

Gangping Yan (Institute of Microelectronics of Chinese Academy of Sciences), Gaobo Xu (Institute of Microelectronics of Chinese Academy of Sciences), Jinshun Bi (Institute of Microelectronics of Chinese Academy of Sciences), Guoliang Tian (Institute of Microelectronics of Chinese Academy of Sciences), Huaxiang Yin (Institute of Microelectronics of Chinese Academy of Sciences), Yongliang Li (Institute of Microelectronics of Chinese Academy of Sciences) and Qiuxia Xu (Institute of Microelectronics of Chinese Academy of Sciences).

Abstract

Total ionizing dose (TID) and transient dose rate (TDR) effects on planar and vertical ferroelectric tunneling-field-effect-transistors (TFET) are investigated using TCAD simulations. First, two types of TFET structures are constructed numerically. Then the electrical properties of these devices are studied under different irradiation doses, demonstrating that they are slightly affected by TID effects, especially for the vertical transistor. The TDR-induced maximum photocurrents in two types of TFETs under different operation voltage and dose rate are extremely small with respect to the conventional bulk transistors. Physical mechanisms of device performance degradation are investigated in detail. The results suggest that the vertical ferroelectric TFET, which shows better electrical performance and radiation-hard characteristics compared with the planar one, is useful for the design of large-scale logic circuits for application in harsh radiation environments. *return*

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52 *Vibration-induced dynamic characteristics modeling of electrical contact resistance for connectors*

Le Xu (Harbin Institute of Technology), Sanqiang Ling (Harbin Institute of Technology), Donghui Li (Harbin Institute of Technology) and Guofu Zhai (Harbin Institute of Technology).

Abstract

The electrical contact resistance (ECR) of connectors fluctuates periodically under vibration stress. However, a theoretical model used to explain the dynamic characteristics of ECR has not been fully proposed. The dynamic characteristics of ECR are presented after an analysis of the measured results. Moreover, according to the Greenwood-Williamson model for elastic contact and the equivalent spring model for random rough surfaces, the change in the contact pressure of electrical connectors during vibration is studied. On this basis, combining with the Holm electrical contact theory, a dynamic model of ECR under vibration conditions is established. The model can theoretically explain the phenomena of ECR found in the experiments. A good correlation between experimental and predicted ECR fluctuation is achieved. *return*

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53 *Damage based PoF model of solder joints under temperature cycling and electric coupling condition*

Jiaxin Yuan (School of Reliability and Systems Engineering, Beihang University, Beijing), Sujuan Zhang (School of Reliability and Systems Engineering, Beihang University, Beijing), Bo Wan (School of Reliability and Systems Engineering, Beihang University, Beijing), Guicui Fu (School of Reliability and Systems Engineering, Beihang University, Beijing) and Maogong Jiang (School of Reliability and Systems Engineering, Beihang University, Beijing).

Abstract

To predict the life of solder joints under temperature cycling and electric coupling condition, this paper proposes a Physics of Failure (PoF) model based on the continuum damage mechanics (CDM). Firstly, considering the effect of current on solder's mechanical properties, the current-affected constitutive models of plastic fatigue and creep are constructed. Then, based on the mechanism of energy dissipation, a unified creep-plasticity damage evolution law is deduced, and the nonlinear accumulation damage model is developed. Choosing electric resistance as the indirect damage variable measurement, the thermal-electric coupling PoF model is finally established by substituting the current-affected constitutive models into the damage evolution model. A thermal-electric coupling test is carried out to verify the accuracy of PoF model. The experimental results confirm that the proposed PoF model can effectively predict the life of solder joints under temperature cycling and electric coupling condition. *return*

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54 *A power transfer model-based method for lithium-ion battery discharge time prediction of electric rotatory-wing UAV*

Diyin Tang (Beihang University (BUAA)), Mengtong Gong (Beihang University (BUAA)), Jinsong Yu (Beihang University (BUAA)) and Xiang Li (Zhongshan Hankun Intelligent Technology Co., Ltd).

Abstract

Abstract – This paper develops a power transfer model-based method to estimate real-time state of energy (SOE) and predict end of discharge (EOD) time of rotatory-wing UAVs lithium batteries under dynamic operational conditions. A discrete-time state-space model of battery is first established to model the process of battery power consumption and establish a mapping of battery unobservable state of energy (SOE) to measurable parameters such as voltage and current. Then a power consumption model of UAV is established based on predetermined flight mission of UAV using aerodynamics and momentum theory, which estimates power consumption of UAV under different operational conditions. Its calculation results can be directly used in battery state-space model as its input. Finally, a Particle Filter (PF) approach with Adam optimization algorithm is developed to estimate SOE and predict EOD time on-line, and better prediction results compared to conventional PF are achieved. Real experiments on UAV verify the effectiveness of the proposed method. *return*

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56 *Analog and Mixed-Signal Circuits simulation for product level EMMI analysis*

Tommaso Melis (Univ. Grenoble Alpes, CNRS, Grenoble INP, TIMA), Emmanuel Simeu (Univ. Grenoble Alpes, CNRS, Grenoble INP, TIMA), Etienne Auvray (ST Microelectronics Grenoble) and Paul Armagnat (ST Microelectronics Grenoble).

Abstract

The goal of this work is to propose a new flow that integrates the analog and mixed signal simulation of the circuits to reproduce the EMMI, as support for the fault localization process. We will explore the emission typologies of the transistors focusing the attention on the DMOS structure. The first experimental results show the benefits of this approach. *return*

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59 *Novel Failure Traces beyond the Barrier on the Floating Device*

Gwang Wook Lee (Samsung Foundry), Sunnu Shim (Samsung Foundry), Wookhyun Cho (Samsung Foundry), Wonse Kim (Samsung Foundry), Kisoo Lee (Samsung Foundry), Jaehyun Kim (Samsung Foundry), Seongjun Cho (Samsung Foundry), Seokjun Won (Samsung Foundry) and Bonyoung Koo (Samsung Foundry).

Abstract

Failure Analysis (FA) on Fully Depleted Silicon On Insulator (FDSOI) device is challenging due to its unique structure with buried oxide layer. Based on the in-depth study on structural limitation of the device, this paper firstly reports novel approaches for the physical and electrical FA methodologies with the success stories for yield learning. Furthermore, we demonstrate the improvements of FA methods compared to the conventional ones and how new ideas are applied to the analysis procedure. *return*

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60 *Microstructure Evolutions upon Ni(Pt) Silicidation and the Different Responses to the Metal Etch*

Wentao Qin (On Semiconductor), Dorai Iyer (On Semiconductor), Jim Steinwall (On Semiconductor), Robert Watkins (On Semiconductor), George Chang (On Semiconductor), Carroll Casteel (On Semiconductor), Jim Morgan (On Semiconductor) and Mike Thomason (On Semiconductor).

Abstract

Different responses of Ni(Pt) silicides to metal etch were interpreted, to enable addressing the underlying processing issue. After metal etch, the layer stack on the wafer silicided at the nominal 400 ?C was Ni(Pt)/Ni2Si(/Si), and flakes appeared on the wafer. With the higher temperature, the extent of the silicidation was greater. The stack on the wafer became Ni-oxide/Si-oxide/(NiPtx)Si/NiSi/Si. There was no flaking issue and the desired etch selectivity was achieved. It is the decomposition of Ni2Si that led to the bi-layer structure of NiSi, and the minimization of free energy that drove the out-diffusion of Ni and Si from the NiSi to form the surface oxides. Ni-oxide formed on Si-oxide because Si-oxide is thermodynamically more stable than Ni-oxide. The two layers of oxides and the density of bond energy of NiSi being higher

than that of Ni2Si made the stack more resistant to the metal etch and resulted in the desired etch selectivity and subsequently solution to the problem. return

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61 *Reliability improvement for palladium coated copper wire using additive element*

Motoki Eto (Nippon Micrometal Corporation), Noritoshi Araki (Nippon Micrometal Corporation), Takashi Yamada (Nippon Micrometal Corporation), Robert Klengel (Fraunhofer Institute for Microstructure of Materials IMWS), Sandy Klengel (Fraunhofer Institute for Microstructure of Materials IMWS), Masaaki Sugiyama (Osaka University) and Shinji Fujimoto (Osaka University).

Abstract

In this paper, we investigate the corrosion behaviour of Cu9Al4 with and without Pd and additive element, clarifying the effect of Pd and additive element on the corrosion resistance of Cu-Al IMC. Furthermore, improving mechanism against pitting corrosion under high temperature storage life test is also discussed with microstructure analysis. The result shows that additive element forms protective passivation layer on the IMC and Cu surface. return

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62 *A rapid life-prediction approach for solder joints based on modified Engelmaier fatigue model*

Yuxiong Pan (CRRC ZHUZHOU INSTITUTE Co., Ltd), Guifa Zhou (CRRC ZHUZHOU INSTITUTE Co., Ltd), Xu Wang (CRRC ZHUZHOU INSTITUTE Co., Ltd) and Fen Kuang (CRRC ZHUZHOU INSTITUTE Co., Ltd).

Abstract

Accelerated life test (ALT) is widely used to predict life of solder joints nowadays, and how to shorten the test time and improve the precise of evaluation is one of the most important issues. Based on statistical results of field failure for solder joints, improved ALT under combined thermal cycling and vibration loading conditions was designed and carried out. This paper presents a modified Engelmaier fatigue model to predict life of solder joints, by taking into account field failure data and ALT testing data. The results show that test time of improved ALT is more shorter than conventional one , and the result of remaining life prediction based on modified Engelmaier fatigue model becomes more precise due to improving life model and increasing information. return

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65 *Thermal Optimized Discontinuous Modulation Strategy for Three Phase Impedance Source Inverter*

Ping Liu (Hunan University), Jie Xu (Hunan University) and Chunming Tu (Hunan University).

Abstract

This paper presents a novel discontinuous space vector modulation (SVM) strategy to reduce the thermal stress of three phase impedance source inverters (ISI). By exploiting the switch clamping mechanism and proper arrangement of the shoot-though (ST) states, the proposed strategy functions to optimize the thermal performance and improve the reliability of ISI. The feasibility of the proposed strategy has been benchmarked by simulation and experiment. More analysis will be provided in the final paper. return

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68 *Reliability test for Subsea Power Semiconductors*

David Guillon (ABB Power Grid Semiconductors), Barbara Scherrer (ABB Power Grid Semiconductors) and Franc Dugal (ABB Power Grid Semiconductors).

Abstract

Following the demand from a new domain of application, a test setup was developed to evaluate the performance of high-power semiconductor device when exposed to a dielectric liquid and high pressure. The specific test conditions were established to emulate the conditions inside a tank place in a deep-sea

environment. Those conditions can be characterized by two key parameters: the pressure and the chosen dielectric/thermal liquid. The power semiconductor device is to be tested at high and low temperature to simulate operation under maximum load as well as when turned off, respectively. The reliability tests outlined here serve to support the development and the validation of Subsea technology for semiconductors power modules. return

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70 *Simplified Hybrid Reliability Simulation Approach of a VSC DC Grid with Integration of an Improved DC Current Flow Controller*

Puyu Wang (Nanjing University of Science & Technology), Song Wang (Department of Electrical Engineering, School of Automation, Nanjing University of Science and Technology), Xiao-Ping Zhang (University of Birmingham), Xin Zhao (Southeast University) and Zhengrong Xiang (Nanjing University of Science and Technology).

Abstract

In this paper, different reliability simulation approaches of an improved DC current flow controller (CFC) integrated voltage-sourced converter (VSC) based DC grids are investigated with the following contributions: (1) In order to achieve bidirectional power flow control and fault current blocking capability, an improved DC CFC topology with a set of reversed switches is proposed to enhance the controllable path and control margins; (2) Two different reliability simulation approaches of the improved DC CFC integrated meshed multi-terminal DC (M2TDC) grid are analysed. In Approach I, the VSCs and their AC sides are modelled without simplification. In Approach II, the VSCs and their AC sides are represented by ideal DC voltage/current sources to simplify the system modelling; (3) Synthesizing the merits of both approaches while avoiding the deficiencies, a hybrid reliability simulation approach is proposed with high efficiency of simulation while maintaining the accuracy; (4) In order to further enhance the simulation efficiency, a different reliability simulation approach of the ideal DC current source, namely improved ideal DC current source, is proposed. Simulation systems are established in PSCAD/EMTDC for verification. return

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71 *Reliability analysis of excitation control modes of a synchronous condenser during grid-integration at the speed-falling stage*

Puyu Wang (Nanjing University of Science & Technology), Tao Yuan (Nanjing University of Science and Technology), Qingwen Mou (Nanjing University of Science and Technology), Wei Gu (Southeast University), Zhengrong Xiang (Nanjing University of Science and Technology) and Zhao Liu (Nanjing University of Science and Technology).

Abstract

As a kind of reactive power compensation equipment, a synchronous condenser has advantages of strong overload capacity and effective suppression of commutation failures. It has been widely used in AC/DC power transmission systems. In this paper, the excitation control modes of the synchronous condenser during grid-integration at the speed-falling stage are studied with three contributions: (1) The necessity of using the exciter at the speed-falling stage and the associated excitation control characteristics are analysed. The dynamic behaviours with different mono-excitation-control modes are compared with identification of the merits and drawbacks. (2) In order to smooth the voltage rising curve during the stator voltage establishment at the speed-falling stage so as to enhance the reliability of starting the synchronous condenser, a sequential hybrid control scheme is proposed with PID controller for excitation at the initial and final stage, and for constant excitation at the middle stage. (3) In order to mitigate the oscillations during grid-integration, a control scheme of pre-insertion of an energy-absorption impedance (EAI) is proposed. The effectiveness and superiority of the proposed sequential hybrid excitation control mode with pre-insertion of an EAI for smoothing the voltage rising curve and mitigation of the oscillations are justified by the simulation results in PSCAD/EMTDC. return

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72 *Comparative evaluation of mission profile based reliability assessment methods of power modules in motor drive inverter*

Ui-Min Choi (Seoul National University of Science and Technology), Ionut Vernica (Aalborg University), Dao Zhou (Aalborg University) and Frede Blaabjerg (Aalborg University).

Abstract

In this paper, the time-dependent reliability of the IGBT module obtained by Monte Carlo method from a certain Bx lifetime is compared with that estimated by the complete percentile lifetime model in the case study of motor drive inverter. The complete percentile lifetime model is developed by the power cycling test results of 30 IGBT modules. *return*

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74 *An Improved Lifetime Prediction Method for Metallized Film Capacitor Considering Harmonics and Degradation Process*

Chunlin Lv (Xi'an Jiaotong University), Jinjun Liu (Xi'an Jiaotong University), Yan Zhang (Xi'an Jiaotong University), Wanjun Lei (Xi'an Jiaotong University) and Rui Cao (Xi'an Jiaotong University).

Abstract

Metallized film capacitor (MFC) is one of the key components in the power electronic converter, accounting for a large proportion of failures. However, the influence of harmonics and degradation process on MFC are not well described by the conventional lifetime prediction method, which leads to a large deviation between prediction result and engineering practice. Therefore, this paper further explores the aging failure mechanisms and proposes an improved lifetime prediction method. The function mechanism that the harmonics change the partial discharge inside MFC to affect lifetime is expounded, which is modelled by several influencing factors. Moreover, the coupling effect of thermal stress and MFC aging is discussed by an improved aging model. The ESR degradation curves obtained from this model are consistent with the experimental results, verifying the validity of this method.

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75 *Capacitive micromachined ultrasonic transducers leak detection by dye penetrant test*

Antoine Nowodzinski (CEA-Leti).

Abstract

Dye penetrant test has been used to detect non hermetic capacitive micromachined ultrasonic transducers (CMUTs). The method has proven its ability to highlight faulty CMUTs among more than hundreds of CMUTs. The fluorescence microscopy image highlights the defective CMUTs with a strong contrast and respecting the shape of the CMUTs, which makes it possible to design robust faulty CMUT automatic identification algorithms. Scanning electron microscopy and focus ions beam (FIB) analysis have been performed in order to check the reliability of the detection of the non-hermetic CMUTs. Observations confirmed the reliability of the method.

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76 *A study of hopping transport during discharging in SiNx films for MEMS capacitive switches*

Dimitrios Birmpiliotis (University of Athens), Matroni Koutsoureli (University of Athens), George Stavrinidis (Foundation for Research and Technology - Hellas (FORTH)), George Konstantinidis (FORTH-IESL-MRG-Heraklion) and George Papaioannou (University of Athens).

Abstract

The impact of effective temperature which combines the effects of ambient temperature and electric field during discharging in MEMS switches is demonstrated for the first time. The aim of the present work is to study the impact of the effective temperature on the hopping conduction parameters which may lead to material optimization and possible exploitation in MEMS switches.

77 *Field emission induced-damage in the actuation paths of MEMS capacitive structures*

John Theocharis (University of Athens), Matroni Koutsoureli (University of Athens), Spiros Gardelis (University of Athens), George Konstantinidis (FORTH-IESL-MRG-Heraklion) and George Papaioannou (University of Athens).

Abstract

The paper analyses for the first time the electrical discharges across the actuation paths in MEMS capacitive structures. Electric fields beyond the field emission region were applied and under different pressure levels below the atmospheric one. The current-voltage characteristics reveal a stable field emission followed by a noisy one and a region of plasma discharge that causes severe damage to actuation paths. Finally, the experimental results reveal a progressive damage with the current increasing. *return*

78 *Ultrasonic monitoring performance degradation of lithium ion battery*

Jae-Yeon Kim (Seoul National University of Science & Technology), Jang-Hun Jo (Seoul National University of Science & Technology) and Jai-Won Byeon (Seoul National University of Science & Technology).

Abstract

To monitor the performance and reliability of a lithium-ion battery during charge/discharge cycles, an ultrasonic time-of-flight (ToF) and attenuation measurement was performed. Ultrasonic ToF of the reflected pulse echo increased with the decrease in the state of charge (SoC) and with the increase in number of cycles (i.e., degradation). A health evaluation map relating SoC with ToF at various cycles was constructed. In this map, ultrasonic hysteresis was reported, of which area reflected the magnitude of irreversible electrochemical damage to the battery material. A linear correlation between the ToF and the number of cycles was observed. *return*

80 *Peculiar Failure Mechanisms in GaN Power Transistors*

Massimo Vanzi (University of Cagliari DIEE) and Giovanna Mura (University of Cagliari DIEE).

Abstract

Commercial GaN power amplifiers, made of a pair of discrete transistors for operation in Doherty configuration, failed during HAST tests. Failure Analysis pointed out a layout-specific issue related to thermal expansion of the field plates. Anyway, the search for initial degradation stages by means of OBIRCH and Emission Microscopy revealed a subtle second mechanism, involving Ga interdiffusion into the gate metal lines, coming from hollow pipes in GaN. Both mechanisms are discussed.

81 *Effect of Thermal and Vibrational Combined Ageing on QFN Terminal Pads Solder Reliability*

Faical Arabi (IMS), Alexandrine Gracia (University of Bordeaux, IMS Laboratory), Jean-Yves Delétage (IMS Laboratory) and Helene Fremont (IMS-Bordeaux).

Abstract

Automotive environment generates vibration and temperature fluctuation, which reduces the life of electronic boards. In this paper, vibration tests are performed continuously throughout thermal cycling to investigate the combined effect of temperature and vibration on the SAC305 solder of Quad Flat No-lead (QFN) terminals pads bonded on Printed Circuit Board (PCB). Experimental results imply that the number of combined cycles affects the PCB responses. Fifty thermal cycles combined with fatigue random vibration test has been carried out on 100 QFN terminal pads solder. Statistical evaluation of the solder fatigue showed that cracking has started in 68% of them. On the other hand, an accurate numerical model for

simultaneous combined thermal cycling and vibration simulation is developed and validated by experiments.

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82 *0.5µm GaN RF power bar technology space evaluation*

Jerome Van de Casteele (United Monolithic Semiconductors), Hannes Stuhldreier (United Monolithic Semiconductors), Diane Bouw (United Monolithic Semiconductors), Cyril Gourdon (United Monolithic Semiconductors), Marianne Raoult (United Monolithic Semiconductors), Erwan Durand (United Monolithic Semiconductors), Sebastien Van Den Berghe (United Monolithic Semiconductors), Marc Hollmer (United Monolithic Semiconductors), Marco Grunwald (United Monolithic Semiconductors), Benoit Lambert (United Monolithic Semiconductors), Herve Blanck (United Monolithic Semiconductors) and Andrew Barnes (European Space Agency).

Abstract

This paper describes the test plan and the main results achieved by UMS during the space evaluation program of its second generation 0.5µm GaN RF power bar technology, so called GH50-20. The technology has successfully passed a space evaluation program. The space evaluation tests results are summarised: A life time higher than 5E+06 hrs @ 200°C is found, SEE, TID and DD radiation hardness safe area were defined, and failure rate below 8 FIT @ 200°C was determined . The results also include demonstration of representative integrated circuits up to 130 W RF power level when operated in L-band in continuous wave (CW) mode. *return*

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83 *Combined Experimental and Numerical Approach for Investigating the Mechanical Degradation of the Interface between Thin Film Metallization and Si-Substrate after Temperature Cycling Test*

Dawei Zhao (Chair of Electron Devices - Friedrich-Alexander University Erlangen-Nürnberg), Sebastian Letz (Fraunhofer Institute for Integrated Systems and Device Technology IISB), Zechun Yu (Fraunhofer Institute for Integrated Systems and Device Technology IISB), Andreas Schletz (Fraunhofer Institute for Integrated Systems and Device Technology IISB) and Martin März (Chair of Energy Electronics - Friedrich-Alexander University Erlangen-Nürnberg).

Abstract

The thin film metallization, as a key structure of the semiconductor devices, realizes the bond-ability of the chips on circuit carriers and directly influences the electrical and mechanical reliability of the interconnection. In a previous study, a recently developed method, cross-sectional nanoindentation (CSN), was utilized in order to characterize the adhesion strength degradation of the thin film metallization and its feasibility was proofed. In this paper, based on the now extended CSN test results from the previous study, a combined experimental and numerical approach with a cohesive zone model (CZM) has been developed in order to evaluate the adhesion strength degradation of the thin film metallization quantitatively by means of the critical strain energy release rate Gc. in order to obtain a measure with physical meaning and extrapolation ability. *return*

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84 *Effects of gamma radiation on suspended silicon nanogauges bridge used for MEMS transduction*

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Abstract

This paper proposes a study on the resilience to radiation of MEMS sensors based on piezoresistive transduction by means of suspended silicon nanogauges. It is particularly interesting for applications in severe environment like in space or in nuclear plant. In order to evaluate their robustness to radiation, sensors have been exposed to 60Co Gamma (γ) rays up to a total dose of 100 kGy with a dose rate of 600 Gy/h. This work shows that the resistivity of a single nanogauge exhibits a sensitivity of 16.5 ppm/kGy whereas the silicon nanogauges bridge used for MEMS transduction is immune to radiation with a variation of – 4 ppm/h, like in normal operation. It is the consequence of the differential measurement at the terminals of the two nanogauges that enables to cancel radiation effects.

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90 *Life-cycle Reliability Design Optimization of High-power DC Electromagnet-ic Devices Based on Time-dependent Non-probabilistic Convex Model Pro-cess*

Xuerong Ye (Harbin Institute of Technology), Hao Chen (Harbin Institute of Technology), Qisen Sun (Harbin Institute Of Technology), Cen Chen (Harbin Institute of Technology), Hao Niu (Harbin Institute of Technology), Guofu Zhai (Harbin Institute of Technology), Wenwen Li (state grid jibei marketing service center(metrology center)) and Ruiming Yuan (state grid jibei marketing service center(metrology center)).

Abstract

Abstract –The life-cycle reliability of high-power DC electromagnetic devices due to multi-source heterogeneous uncer-tainties in the design, manufacturing, loads, degradation and cumulative damages has become increasingly prominent, life-cycle reliability optimization has attracted extensive attention. The design optimization strategy based on reliability, which combines the static/time-independent hypothesis and random theory, is inapplicable to life-cycle design optimiza-tion. Therefore, a time-dependent uncertainty analysis and life-cycle quality reliability optimization method are proposed in this study. Based on the information entropy transformation method, the fuzzy uncertainty is transformed into a proba-bility density function of equivalent random variables, and intervals for the random variables are determined in the stand-ard normal space. In this way, the heterogeneous uncertainty is unified as an interval type. Moreover, the time-dependent characteristics of the uncertainty parameters are transformed into a time-dependent of the characteristics through ellip-soidal model process. A life-cycle expression method based on an orthonormal basis is proposed to form a life-cycle time-dependent non-probabilistic convex model process. Therefore, the analytical expression of out-crossing rate in which there are many non-probabilistic convex model process parameters are derived and the corresponding upper and lower bounds of out-crossing rate can be obtained. Then, a life-cycle reliability design optimization model is constructed and the optimal solution is determined from intelligence algorithm. The effectiveness of proposed method was verified by a high-power DC electromagnetic relay in renewable energy systems. *return*

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91 *Research on 3D NAND flash reliability from the perspective of threshold voltage distribution*

Debao Wei (Harbin Institute of Technology), Hua Feng (Harbin Institute of Technology), Xiaoyu Chen (Harbin Institute of Technology), Liyan Qiao (Harbin Institute of Technology) and Xiyuan Peng (Harbin Institute of Technology).

Abstract

Aiming at the inaccurate problems of lifetime prediction and reliability evaluation of 3D TLC NAND flash memory, a method to evaluate the remaining lifetime and the reliability of flash memory based on the threshold voltage distribution is proposed. In order to analyze the impact on Program/Erase (P/E) cycles on the flash memory from the perspective of voltage distribution, a complete distribution curve of threshold voltage is drawn from the construction of a reasonable mathematical model. The P/E cycles has always been regarded as an important indicator to evaluate the reliability and remaining lifetime of flash memory. Currently, most evaluations of flash memory reliability and lifetime expectancy are based on the relationship between the P/E cycles and the raw bit error rate. The bit error distribution of TLC flash memory is not uniform, and there is a clear centralized distribution phenomenon, which will easily exceed the controller's error correction capability, and then affect the reliability of the flash memory. Therefore, it is not accurate to analyze the reliability of the flash memory only based on the bit error rate. Analyzing the

reliability and lifetime expectancy of flash memory from the perspective of threshold voltage is a more reliable and more essential method, however, there is almost no literature to do this research. In order to analyze the impact on P/E cycles on 3D TLC NAND flash memory from the perspective of threshold voltage distribution, two methods to draw the threshold voltage distribution curve and compare them are given below. First, we obtain the origin test data from our hardware-software co-design experimental platform for 3D NAND flash. Fig. 1 shows a photograph of our 3D NAND flash experimental platform. This experimental platform primarily consists of the processor (Zynq) and a NAND flash array. We select MT29F256G08EBHAF, which is a 3D TLC NAND flash from Micron Inc.. In the first method, the read offset function of the flash memory is used to control 7 read reference voltages so that the "voltage window" of the 8 cell states of the flash memory is controlled.Therefore, the threshold voltage distribution functions of all states of the TLC flash are obtained. Then, a complete distribution model of threshold voltage is drawn through a series of operations such as misalignment, model fitting, and state merging(see Fig. 2). In the second method, by virtue of the large amount of obtained flash memory data, the data status of the cells that have read errors are counted (see Fig. 3). In order to calculate an overlapping area of the adjacent status, the counts of jump direction of the error bits is given. Finally, a reasonable distribution model for statistic is fitted (see Fig. 4). Two methods of drawing the threshold voltage distribution are investigated. A completed distribution of the threshold voltage in almost all voltage ranges is obtained in the first method. In the second method, a smaller amount of calculation is done compared to the first method. While the distribution curve can accurately restore the overlapping area of adjacent status. After plotting the initial distribution of threshold voltage, the continuous P/E operations on the flash memory are performed. At 100, 500, 1000, 2000, 5000, and 10,000 P/E cycles, these two methods are used to draw the distribution curve of threshold voltage. The distribution curve of threshold voltage for 100~10,000 P/E cycles is drawn by the read offset method of 3D TLC NAND flash memory (see Fig. 5(a)). Three observations are presented from this figure. (1) The threshold voltage gradually shifts to the left as the number of P/E cycles increases. (2) The divergence of the threshold voltage distribution increases. (3) Bit errors mostly occur in P3 and P4 states. The overlapping area method was used to process the same data and draw a distribution curve (see Fig. 5(b)). Investigating the Figure 5, the same conclusions are drawn as Figure. 5(a). Combining these two methods, the P/E cycles-overlap area conversion formula is obtained. According to this formula, the lifetime prediction of the flash memory can be performed. And by comparing the overlapping area of adjacent areas, the strength of the error correction algorithm required for the corresponding page can be obtained. Compared with the conventional used curve of P/E cycles-error rate, it reflects the most concentrated part of the flash memory error rate and makes lifetime prediction more accurate. *return*

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92 *A fault tolerant switched reluctance motor drive for electric vehicles under multi-switches open-fault conditions*

Qingqing Yang (Hefei University of Technology), Rui Wang (Hefei University of Technology), Mingyao Ma (Hefei University of Technology), Shuying Yang (Hefei University of Technology) and Xing Zhang (Hefei University of Technology).

Abstract

Abstract –A power converter with effective fault-diagnosis and fault-tolerant control can improve the reliability of switched reluctance motor drive system (SRD). At present, there are many research results on single power switch fault. In view of the multi-switches faults caused by the harsh operational environments and repetitive duty cycles, this paper presents a flexible fault-tolerant topology with fault-diagnosis, fault-tolerant control strategy for diverse open-circuit faults occurring in the SRD under different working conditions, and the common H-bridge has been selected as the fault-tolerant topology. When the SRD is subjected to open-circuit faults, the fault-diagnosis can be achieved by detecting the characteristic of the real-time phase currents, and then the faulty switches can be replaced automatically by the corresponding reverse ones to sustain the driving operation with further optimized output torque. *return*

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93 *A high-efficiency threshold voltage distribution test method based on the reliability of 3D NAND flash memory*

Debao Wei (Harbin Institute of Technology), Xiaoyu Chen (Harbin Institute of Technology), Hua Feng (Harbin Institute of Technology), Liyan Qiao (Harbin Institute of Technology) and Xiyuan Peng (Harbin Institute of Technology).

Abstract

With the improvement of manufacturing technology and the use of multi-level technology, the amount of charge stored in a flash memory cell decreases, the number of bits stored in each cell increases, the threshold voltage window becomes smaller. Therefore, it is more vulnerable to external interference to cause the overlap of threshold voltages between adjacent states, which makes it difficult to determine the logical value of cell, resulting in the decline of NAND flash memory reliability. Exploring and modelling the threshold voltage distribution of NAND flash and its changes due to various factors can help us to understand how the raw bit error occurs, and design an efficient mechanism to improve the reliability of flash memory. In this paper, we obtain the origin test data from our hardware-software co-design experimental platform for 3D NAND flash. Fig. 1 shows a photograph of our 3D NAND flash experimental platform. This experimental platform primarily consists of the processor (Zynq) and a NAND flash array. We select MT29F256G08EBHAF, which is a 3D TLC NAND flash from Micron Inc.. The experimental flash chip provided the READ OFFSET function which can offset the read reference voltage to obtain the threshold voltage distribution functions of each state. After that, a complete threshold voltage distribution can be drawn through misalignment and state merging. Based on the platform, we tested the advantages and disadvantages of two statistical methods of threshold voltage, and then used the better one to explore the threshold voltage distribution when programming different test sets into the block. 1. TLC flash has 8 storage states with a read reference voltage between two adjacent states, as shown in Fig. 2. In this paper, we call the pages affected by the offset read reference voltage as the affected pages. It can be seen that no matter what data is written, such as the sequence of full 0 or full 1 bits (see Fig. 3), or the random sequence in Fig. 4, the threshold voltage distribution obtained by only counting the bits error of affected page is the same as that obtained by counting the bits error of a group of shared pages. While only counting the affected page can save two thirds of the time. In our experiment, if only the bits error of affected pages were counted, the platform would cost 662021658 μs, while 1986083873 μs is needed for the all state statistics. 2. Due to the severe inter-cell interference in NAND flash, writing different test sets will lead to different threshold voltage distributions. When cells on the same byte line are written to the same data but cells on adjacent byte lines are written differently, the flip rate between P3 state and P4 state is the highest. Figure 5 shows the threshold voltage distribution when the cell state of adjacent word line is fixed, while Figure 6 shows the cell state of adjacent word line when it is random. It can be seen that when there is only interference between the word lines, most errors are caused by the LSB (Least Significant Bit) flip. When cells on adjacent bit lines are programmed into different data, and cells on the same bit line are written into the same one, it can be observed in Fig. 7 that the threshold voltage distribution of each state is more concentrated than when the cells in a word line store the same data. When the cells on adjacent word lines and adjacent bit lines are written with different data, the threshold voltage distributions of the three storage states whose LSB bit stores '1' are the same when different data is written into the adjacent word lines. And the threshold voltage distribution of the four states with the LSB bit of '0' shifts to the right, so that their threshold voltages are almost within the voltage window separated by the read reference voltage, thereby reducing the error rate. To sum up, this paper puts forward a statistical method of threshold voltage distribution that only counts the bits error of affected page, which can shorten the statistical time by two thirds while ensuring the accuracy. Using this method, we explore the threshold voltage distribution of three different data sets. And finally find that when interference mainly comes from adjacent word lines, the LSB flip will occur. When there is programming interference between the adjacent bit lines of the same word line, the threshold voltage distribution of each state will be more concentrated.. When programming interference exists between the adjacent word lines and the adjacent bit lines, the threshold voltage distribution of the cells with the LSB of '0'will shift to the right. *return*

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95 *Lithium-ion Battery Performance Degradation Evaluation in Dynamic Operating Conditions based on a Digital Twin Model*

Xinpeng Qu (Harbin Institute of Technology), Datong Liu (Harbin Institute of Technology), Yuchen Song (Harbin Institute of Technology), Xiuhai Cui (Harbin Institute of Technology) and Yu Peng (Harbin Institute of Technology).

Abstract

The performance of lithium-ion batteries degrades over time. Evaluating the performance degradation for lithium-ion batteries is essential to ensure the operational reliability and reduce the risk of host-system downtime. The battery capacity that is obtained by completely charging and discharging a battery cell,

reflects the reliability of a lithium-ion battery. But in practical applications, the battery is dynamically charged and discharged. This makes it difficult to measure the actual capacity and further evaluate battery performance degradation. This paper proposes a performance degradation evaluation model by estimating the battery actual capacity in dynamic operating conditions. A health indicator (HI) that is extracted from the measurable parameters to reflect the battery performance degradation. A battery digital twin model that describes the relationship between the cell voltage and the cell state-of-charge (SOC) are modelled by the long short-term memory (LSTM) algorithm, which takes the HI as a temporal measurement. The battery actual capacity can be obtained by virtually completely discharging this digital twin model. The experimental results illustrate the potential of the proposed method applying in dynamic operating conditions.

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97 *Short-circuit and open-circuit faults monitoring of IGBTs in SST using collector-emitter voltage*

Qiuling Cao (Key Laboratory of Smart Grid of Ministry of Education, Nankai District, Tianjin University, Tianjin 300072), Yanbo Che (Key Laboratory of Smart Grid of Ministry of Education, Nankai District, Tianjin University, Tianjin 300072), Jianxiong Yang (Key Laboratory of Smart Grid of Ministry of Education, Nankai District, Tianjin University, Tianjin 300072) and Menglai Mi (Key Laboratory of Smart Grid of Ministry of Education, Nankai District, Tianjin University, Tianjin 300072).

Abstract

Aging and malfunction of devices with great power has been the main cause of the grid system's collapse and failure. Being frequently used in the grid system, the failure of SST has a great impact on the energy-saving and normal operation of the network system. Moreover, the main switching element of SST is IGBT of welding type which is also the most fragile part. We firstly introduce the structure and basic function of SST. Then we can conclude the main cause of the converter's internal fault in SST from the phenomenon of uneven current flow in simple paralleled IGBT models. Analyze the changing trend of equivalent resistance of single-phase SST under short-circuit or open-circuit condition, taking the numbers of IGBT in failure mode and the fault type as variables. External electrical parameters of SST change with the failure condition of internal IGBT devices, therefore, voltage and current values will change due to the variation of equivalent resistance. So, propose that the collector-emitter voltage can be used to characterize SST's fault conditions, then establish the simulation model of SST and set different failure circumstances to verify the hypothesis in the simulation process. Eventually, the conclusion can be drawn as follows: the collector-emitter voltage as well as VM which is the voltage of the transformer's primary side in SST can be used to characterize the failure condition of SST's internal converter. *return*

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98 *Investigation of the mechanical properties of corroded sintered silver layers by using Nanoindentation*

Elisabeth Kolbinger (Fraunhofer Institute for Reliability and Microintegration), Simon Kuttler (Fraunhofer Institute for Reliability and Microintegration), Stefan Wagner (Fraunhofer Institute for Reliability and Microintegration) and Martin Schneider-Ramelow (Technical University Berlin).

Abstract

The aim of this study is to gain a better understanding of the behaviour of sintered silver layers for e.g. power electronic applications in corrosive environments. It explicitly deals with the influence of corrosion products on the mechanical properties using Nanoindentation measurements. In addition to these measurements, analytical investigations and porosity analyses are performed. Existing studies mainly deal with the investigation of unaged sintered silver layers or the influence of thermomechanical ageing on the mechanical properties. In contrast, this study focuses on the investigation of the influence of moisture on the mechanical properties of sintered silver. The results show that an increased Young's modulus can be detected by Nanoindentation measurements on corrosion-stressed sintered silver. In addition, increased indentation hardness is also determined. Besides the already known influences on the Young's modulus, a significant influence on the corrosion pattern of the sintered silver layers can be shown. The results are discussed with regard to a filled pore system of the samples. *return*

102 *Multiple Failure Modes Identification of SiC planar MOSFETs in Short-circuit Operation*

Bixuan Wang (Xi'an Jiaotong University), Jingcun Liu (Xi'an Jiaotong University), Wanping Li (Xi'an Jiaotong University), Guogang Zhang (Xi'an Jiaotong University), Yingsan Geng (Xi'an Jiaotong University) and Jianhua Wang (Xi'an Jiaotong University).

Abstract

This paper aims to identify and distinguish multiple failure modes of SiC planar MOSFETs under different SC conditions, based on the transient temperature estimation of two key zones, i.e. the JFET region and the source Al layer adjacent to the upper side of gate dielectric. A multi-layer thermal model is proposed to reproduce the temperature profile, and it has been validated at wide DC bus voltages (from 200 to 800 V). The model is also able to predict the failures using normal SC turn-off waveforms. *return*

104 *Surge Current Capability of Ultra-Wide-Bandgap Ga2O3 Schottky Diodes*

Cyril Buttay (Universite de Lyon, INSA de Lyon, CNRS, Laboratoire Ampere,), Hiu-Yung Wong (San Jose State University, San Jose, CA, USA), Boyan Wang (Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA), Ming Xiao (Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA), Christina DiMarino (Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA) and Yuhao Zhang (Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA).

Abstract

Ga2O3 is an emerging ultra-wide-bandgap semiconductor material offering superior power material limits over Si, SiC, and GaN as well as the availability of large-diameter wafers growing from its own melt. However, Ga2O3 device performance may be limited by the relatively poor thermal conductivity of the material.

In this paper, we investigate the behavior of Ga2O3 Schottky diodes in the condition of forward current surge to explore their electro-thermal ruggedness and the related thermal management. An analytical electro-thermal device model is calibrated with experimental devices and TCAD simulations. Then this device model is incorporated into a SPICE electro-thermal network model, which is used to simulate the device temperature rise during the surge transient, considering various device and packaging configurations (i.e. various chip thicknesses and chip orientations).

It is found that providing heat is removed from the junction side, a Ga2O3 Schottky diode offers a robustness to surge current exceeding that of a SiC Schottky diode. The low thermal conductivity of Ga2O3 is found to be overcome by the enhanced heat extraction from junction-side cooling as well as the the intrinsically small temperature dependence of the on-resistance (and conduction loss) of Ga2O3 devices. *return*

105 *Role of the AlGaN barrier on the long-term gate reliability of power HEMTs with p-GaN gate*

Andrea Natale Tallarico (University of Bologna), Niels Posthuma (imec), Benoit Bakeroot (imec), Stefaan Decoutere (imec), Enrico Sangiorgi (University of Bologna) and Claudio Fiegna (University of Bologna).

Abstract

Forward gate constant voltage stress (CVS) has been performed on 200 mm GaN-on-Si HEMTs with p-GaN gate, processed by imec with different gate process splits. In particular, the adoption of devices with a different magnesium (Mg) concentration, aluminum percentage (Al%) and AlGaN barrier thickness, allowed us to identify the degradation of the AlGaN barrier as responsible for time dependent gate breakdown at room temperature. In particular, lowering Al% and Mg concentration leads to a longer gate lifetime, while an optimum AlGaN barrier thickness is identified at given Al%. *return*

106 *Analysis of the successive breakdown statistics of multilayer Al2O3/HfO2 gate stacks using the time-dependent clustering model*

Jordi Muñoz Gorriz (Universitat Autonoma de Barcelona), Mireia Gonzalez (IMB-CNM), Francesca Campabadal (IMB-CNM), Jordi Suñe (Universitat Autonoma de Barcelona) and Enrique Miranda (Universitat Autonoma de Barcelona).

Abstract

The successive oxide failure statistics theory that arises from the clustering model is used for modelling the ordered time-to-breakdown distributions of Al2O3/HfO2-based nanolaminates. This gate dielectric stack in MIS structures is intended to combine a high injection barrier material (Al2O3) with a high-K material (HfO2). This report demonstrates that the theory of uncorrelated events succesfully describes the breakdown statistics up to the order 15th and allows identifying the origin of the deviation from the standard Weibull model occurring at the high percentiles in the large spread exhibited by the initial leakage current. *return*

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107 *Coupled simulations for lifetime prediction of board level packages encapsulated by thermoset injection moulding based on the Coffin-Manson relation*

Romit Kulkarni (Hahn-Schickard), Mahdi Soltani (IFM, University of Stuttgart), Simon Krafft (IFM, University of Stuttgart), Tobias Groezinger (Hahn-Schickard) and André Zimmermann (IFM, University of Stuttgart and Hahn-Schickard).

Abstract

A fibre orientation dependant material model of the thermoset is implemented to predict the lifetime of electronic components as a part of 2nd level encapsulated packages. Experimental data are used in combination with coupled simulations (process simulation – fibre orientation dependant material model – thermo-mechanical simulation) for defining this lifetime prediction model. An already existing lifetime prediction model based on the Coffin-Manson relation is used initially to evaluate the prediction accuracy. The prediction model is then adjusted and fitted for the current application. *return*

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108 *New definition of critical energy for SiC MOSFET robustness under short circuit operations: the repetitive critical energy*

Cheng Chen (SATIE laboratory – ENS Paris-Saclay - UMR CNRS 8029 – France), Tien Anh Nguyen (SATIE laboratory - CNAM – UMR CNRS 8029 - France), Denis Labrousse (SATIE laboratory - CNAM - UMR CNRS 8029 – France), Stéphane Lefebvre (SATIE laboratory - CNAM - UMR CNRS 8029 – France), Cyril Buttay (Ampère laboratory, Université Claude Bernard Lyon 1, INSA-Lyon, ECL, CNRS, 69622 Villeurbanne, France) and Hervé Morel (Ampère laboratory, Université Claude Bernard Lyon 1, INSA-Lyon, ECL, CNRS, 69622 Villeurbanne, France.).

Abstract

Previous research showed that Si devices could sustain a large number of Short Circuit (SC) events, as long as the energy dissipated during SC remains slightly below a given threshold (the so-called critical energy). In this paper, we show that this is not necessarily true for SiC MOSFETs, which can only withstand a few such SC events. This low robustness to repetitive short-circuit events is related to the gate degradation due to the cumulative carrier injection and leakage currents in the oxide. To ensure safe operation over a large number of SC events, we introduce a new parameter: the “repetitive critical energy”, which corresponds to a SC energy low enough to avoid excessive temperature increase and so to limit the transient gate leakage current during SC events. Below this repetitive SC energy value, the SiC device is able to sustain a large number (more than 1000) of SC events. *return*

109 *Gate leakage current sensing for in situ temperature monitoring of p-GaN gate HEMTs*

Alessandro Borghese (University of Napoli Federico II), Michele Riccio (University of Naples Federico II), Giorgia Longobardi (Dept. of Engineering Cambridge University Cambridge), Luca Maresca (University of Naples Federico II), Giovanni Breglio (University of Naples Federico II) and Andrea Irace (University of Naples Federico II).

Abstract

In this paper, an effective, yet simple, methodology for the temperature monitoring of voltage-driven p-GaN HEMTs based on gate leakage current sensing is presented. The proposed solution has been verified by SPICE ET simulations and experiments on commercial devices within and out of safe operating area (SOA). Moreover, the monitoring circuit can be effectively adopted for commercially available normally-off p-GaN HEMTs with no need of modifying the recommended gate driver circuit. *return*

110 *Combined Experimental-FEM Investigation of Electrical Ruggedness in Double-Sided Cooled Power Modules*

Ciro Scognamillo (Department of Electrical Engineering and Information Technologies, University of Naples Federico II), Antonio Pio Catalano (Department of Electrical Engineering and Information Technologies, University of Naples Federico II), Philippe Lasserre (DEEP Concept, Pau, FR), Cyrille Duchesne (DEEP Concept, Pau, FR), Vincenzo d'Alessandro (Department of Electrical Engineering and Information Technologies, University of Naples Federico II) and Alberto Castellazzi (Faculty of Engineering, Kyoto University of Advanced Science (KUAS), Kyoto, Japan).

Abstract

In this paper, an experimental and numerical study of the electrical ruggedness of double-sided cooled power modules is presented. In particular, the analyses are focused on the role of the spacing between substrates, which are commonly kept distant to avoid electrical failures. To this aim, many samples of such modules were manufactured and tested. FEM electrostatic simulations were performed in COMSOL Multiphysics to provide an explanation of the counterintuitive experimental findings. *return*

113 *Modular dynamic pulse stress test system for discrete high power semiconductors*

Konstantinos Patmanidis (KAI GmbH), Michael Glavanovics (KAI GmbH), Angelos Georgakas (KAI GmbH) and Annette Muetze (TU Graz).

Abstract

The main objective of this paper is to demonstrate the implementation of different dynamic stress test methods within a unified stress test apparatus by retaining most of the functional modules constant and merely change the DUT (Device Under Test) for a variety of power devices and stress patterns. A prototype has been constructed which is capable of implementing SC (Short Circuit) and UIS (Unclamped Inductive Switching), as well as DP (Double Pulse) testing for stressing power semiconductor devices of different voltage and current classes. Last but not least, a protection circuit has been incorporated to safely turn-off the power circuit in case of DUT failure. *return*

115 *Thermo-Mechanical Assessment of Silver Sintering for Attaching Power Components in Embedded PCB*

Faical Arabi (VEDECOM Institute), Toni Youssef (VEDECOM Institute), Martin Coudert (VEDECOM Institute), Gérard Coquery (VEDECOM Institute), Nadim Alayli (VEDECOM Institute), Donatien Martineau (Safran Tech, Electrical & Electronic Systems Research Group) and Olivier Belnoue (ELVIA PCB).

Abstract

PCB-Embedding technology in an established approach for the miniaturization of electronic systems and modules. Silver sintering, which is a reliable alternative to Lead-Free Bonding, is used to assemble the embedded power components in the PCB. Thermal cycles [−25°C/+125°C] have highlighted degradations in the die attach solder. The shear strength of dice decreases from 4 MPa before cycling to 2 MPa at 1040 cycles. The junction temperature has drifted during cycling especially at high temperatures. Simulations have shown that the maximal stresses are in the preg materials. This suggests cracks of the preg during the experiments. Simulations showed also a concentration of plastic stresses on the die attaches. The accumulation of stresses increases during ageing. The presented methodology of thermal cycling simulation represents a good way to estimate the lifetime of Embedded PCB. *return*

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117 *A time-domain stability analysis method for LLC resonant converter based on Floquet theory*

Hong Li (Beijing Jiaotong University), Ying Zou (Beijing Jiaotong University), Xiaheng Jiang (Beijing Jiaotong University) and Chen Liu (Beijing Jiaotong University).

Abstract

This paper establishes the closed-loop time-domain model for LLC resonant converter, and the stability analysis method based on Floquet theory is applied to LLC resonant converter for the first time. The closed-loop stability of LLC resonant converter is analysed according to the eigenvalues of the state transfer matrix of the model, and the stability range of control parameters are obtained. The accuracy and effectiveness of the stability analysis based on Floquet theory are verified by simulation platform in PSIM. Thus, a novel time-domain stability analysis method is provided for LLC resonant converter. *return*

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118 *Asynchronous early output majority voter and a relative-timed asynchronous TMR implementation*

P. Balasubramanian (Nanyang Technological University), Douglas Maskell (Nanyang Technological University) and Nikos Mastorakis (Military Institutes of University Education (ASEI), Hellenic Naval Academy).

Abstract

This paper presents a new asynchronous early output 3-input majority voter that is used to realize a high-speed, low power and less area occupying relative-timed asynchronous TMR implementation. The proposed majority voter is used to realize an example asynchronous TMR implementation, and similar asynchronous TMR implementations were realized using existing asynchronous majority voters. The dual-rail code was used for data encoding and two kinds of four-phase handshaking were considered for data communication. Compared to the best of the existing implementations, on average, we find that the proposed majority voter leads to an efficient asynchronous TMR implementation by simultaneously reducing the cycle time, silicon area, and average power dissipation by 25.1%, 7.5% and 7.8% respectively. The implementations used a 32/28nm CMOS technology. *return*

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119 *Robustness Evaluation Of PCB-Embedded Power Dies Using Solderless Pressed Metal Foam*

Said Bensebaa (Laboratory SATIE), Mounira Berkani (SATIE - UPEC), Stephane Lefebvre (SATIE - Cnam) and Mickael Petit (SATIE - Cnam).

Abstract

This paper presents reliability analysis of an innovative process of embedding power dies in PCBs. Firstly, a description of this solderless package is given. Secondly, experimental investigations of thermal aging for the proposed package are performed through passive thermal cycling in the range of PCB standards. Then 3D simulation model of the package is created using material properties obtained from thermo-mechanical characterizations which realized in previous studies. *return*

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120 *Remaining Useful Lifetime estimation for Electronic Power modules using an analytical degradation model*

Mohamad Nazar (Mitsubishi Electric Research and Development Center Europe (MERCE) & SATIE Lab., Gustave Eiffel University), Ali Ibrahim (SATIE Lab., Gustave Eiffel University), Zoubir Khatir (SATIE Lab., Gustave Eiffel University), Nicolas Degrenne (Mitsubishi Electric Research and Development Center Europe (MERCE)) and Zeina Al-Masry (FEMTO-ST Institute, Univ. Bourgogne Franche-Comté).

Abstract

Power electronic modules undergo electro-thermal stresses due to power losses that lead to several kinds of degradations, and finally to failure. In order to prevent power electronic modules failure, one should assess its reliability in real-time operation. For this purpose, Prognostics and Health Management (PHM) approach could be a promising tool for reliability evaluation. In this paper, we propose an analytical model that describes the metallization to wire-bond contact degradation, which is a main cause that leads the IGBT power module to fail. The usual aging indicator of such damages is the collector-emitter voltage (V_CE) that increases with degradation. The analytical model is related to this indicator and it is based on the contact resistance theory and constriction current lines. The proposed model is hence used to build a prognostic model for estimating the remaining useful lifetime (RUL) of IGBT power modules. The prognostic model is illustrated using aging data coming from accelerated power cycling tests with different stress conditions. Results show a prognostic capability. *return*

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123 *System-level Reliability Assessment for a Direct-drive PMSG Based Wind Turbine with Multiple Converters*

Shuaichen Ye (Beijing Institute of Technology), Dao Zhou (Aalborg University) and Frede Blaabjerg (Aalborg University).

Abstract

System-level reliability of the wind power converter has an essential effect on the operation performance and lifespan of a wind turbine system. In this paper, a wind turbine equipped with a 2 MW direct-drive permanent-magnet synchronous generator (PMSG) serves as a case study. Considering the maximum stator current limitation of the PMSG, several multiple-converter structures and their reliability block diagrams (RBDs) are constructed for the machine side converter (MSC). To investigate the reliability influence caused by the amount of semiconductor components and the current for each components, structures with four and five bridges in parallel are both configured. Reliability evaluation between two major parallel structures, namely, bridges in parallel and converters in parallel are also compared. A detailed discussion regarding the system reliability cumulative distribution function (CDF) is presented, which could serve as reference for further MSC structure design. *return*

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125 *Reliability Prediction of FinFET FPGAs by MTOL*

Emmanuel Bender (Ariel University), Joseph B. Bernstein (Ariel University) and Alain Bensoussan (Thales Alenia Space).

Abstract

Abstract – The MTOL (Multi-Temperature Operational Life) testing method was implemented on FPGA boards from Xilinx 16nm FinFET technology using non-aggressive stress conditions. The study shows that, compared to HCI and EM, BTI is the dominant mechanism. The testing shows a slight, linear increase in degradation with the increase of frequency. Strong evidence shows that the effect is due to self-heating of

the Fins. The temperature increase, due to current induced self-heating caused by high frequency, was tested up to 1 GHz and extrapolated to 3 GHz. The results of this study have significant implications in that we fully characterize the total reliability of FinFET devices over their lifetime. return

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126 *Conducted EMI mitigation in transformerless PV inverters based on intrinsic MOSFET parameters*

Kraiem Sana (LATIS- Laboratory of Advanced Technology and Intelligent Systems), Hamouda Mahmoud (Electric Energy Conversion and Power Electronics CRC-EECPE, ETS de Montréal) and Ben Hadj Slama Jalel (LATIS- Laboratory of Advanced Technology and Intelligent Systems).

Abstract

This article proposes a design methodology that permits the electronic circuit designers to reduce Electromagnetic Interferences (EMI) in power converters, which use a large number of semiconductors. In this work, an identification process of disturbance sources (disturbing cell) is presented. Therefore, the effects of intrinsic source parameters on conducted EMI are investigated to assess the robustness and reliability of the Si-MOSFETs in terms of Electromagnetic Compatibility (EMC). Using a transformerless H5photovoltaic (PV) inverter and by considering the S5 transistor as a source of disturbance, a comparison between the EM signatures given by the effect of different Si- MOSFET references on conducted EMI mitigation is carried out. Furthermore, parasitic elements of interferences propagation paths are employed in order to estimate the high-frequency model which is required for numerical simulations. Experimental results are presented and analyzed. return

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127 *Heavy ion track straggling effect in single event effect numerical simulation of 3D stacked devices*

Tianqi Liu (Department of Computer Science and Technology, Tsinghua University), Dongqing Li (Institute of Modern Physics, Chinese Academy of Sciences), Chang Cai (Institute of Modern Physics, Chinese Academy of Sciences), Peixiong Zhao (Institute of Modern Physics, Chinese Academy of Sciences), Chen Shen (Cogenda Company Ltd), Jie Liu (Institute of Modern Physics, Chinese Academy of Sciences) and Guangwen Yang (Department of Computer Science and Technology, Tsinghua University).

Abstract

Numerical simulation of single event effect in 3D stacked NMOS transistor, inverter and 6T SRAM cell models were conducted using Geant4 and TCAD combined technology. Heavy ion track straggling effect was observed and verified in 3D stacked transistor and inverter models by comparing the ion induced transient pulses and ion striking positions, which is much more significant for low energy heavy ions than high energy counterparts. For large scale simulation of upset sensitive area imaging in stacked 6T SRAM cell model, the result showed that the utilization of lots of heavy ions striking is able to remove the ion track straggling effect. return

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128 *Investigation of critical parameters in power supplies components failure due to electric pulse*

Laurine Curos (CEA-Gramat / IMS Laboratory), Tristan Dubois (Univ. Bordeaux, IMS Laboratory), Guillaume Mejecaze (CEA (Atomic Energy Commission) Gramat), Frédéric Puybaret (CEA (Atomic Energy Commission) Gramat), Bernard Plano (IMS Laboratory) and Jean-Michel Vinassa (Bordeaux INP, IMS Laboratory).

Abstract

This paper presents the influencing parameters for the destruction of power supplies components such as rectifier bridge and rectifier diode, under electric pulse injection. A generator able to inject conducted electric pulses of several hundreds of amperes and a hundred of volts has been designed and used to determine the failure thresholds. These tests permit to show that rectifier bridges destruction follows a

Wunsch and Bell law in current and in power according to the injection duration (t^-1/4 or t^-1/2). Concerning the rectifier diodes, the avalanche breakdown is responsible of the destruction.

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129 *Monitoring of Parameter Stability of SiC MOSFETs in Real Application Tests*

Markus Sievers (KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH), Bettina Findenig (KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH), Michael Glavanovics (KAI Kompetenzzentrum Automobil- und Industrieelektronik GmbH), Thomas Aichinger (Infineon) and Bernd Deutschmann (IFE TU Graz).

Abstract

The goal of this work is to demonstrate the feasibility and challenges with monitoring parameter stability of power semiconductors that are soldered into application relevant stress test hardware. This paper provides an overview of the test system developed for accelerated stress testing under application relevant test conditions. The authors provide an insight into the challenges associated with monitoring parameter stability within such a test system and describe the current solution. The general conclusion is that the presented system is capable to correctly monitoring device parameter stabilities and is capable of stressing SiC MOSFETs with accelerated application relevant test conditions. *return*

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132 *A novel accelerated life-test method under thermal cyclic loadings for electronic devices considering multiple failure mechanisms*

Yaqiu Li (China Electronic Product Reliability and Environmental Testing Research Institute), Guangze Pan (China Electronic Product Reliability and Environmental Testing Research Institute), Qian Li (China Electronic Product Reliability and Environmental Testing Research Institute), Chunhui Wang (China Electronic Product Reliability and Environmental Testing Research Institute) and Xianghong Hu (China Electronic Product Reliability and Environmental Testing Research Institute).

Abstract

A novel accelerated test method has been developed and applied to estimate the lifetime of system-level electronic devices that bear more than one potential failure mechanisms. Firstly, thermal cyclic tests with conditions of temperature extremums and cyclic impact stress are designed to stimulate multiple failures simultaneously. Then, improvements are made in several aspects such as the lifetime distribution of the product, underlying life-stress relationship, and the temperature dependence of the basic acceleration model. Afterward, a comparison of the acceleration model between the proposed and traditional method is conducted by simulation, the results indicate that the proposed model has an advantage in reflecting the failure mechanisms which are sensitive to the low-temperature condition. Finally, real accelerated tests are employed on the custom-circuit samples and the data analysis shows that our method can effectively stimulate multiple failure mechanisms of electronic devices while ensuring the accuracy of the reliability and lifetime assessment. *return*

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133 *A study of material stoichiometry on charging properties of SiNx films for potential application in RF MEMS capacitive switches*

Matroni Koutsoureli (Physics Department, University of Athens), Dimitrios Birmpiliotis (University of Athens) and George Papaioannou (University of Athens).

Abstract

This work presents an in depth investigation regarding the effect of PECVD silicon nitride (SiNx) stoichiometry on its charging properties. The investigation took place in SiNx dielectric films with different Si-content (x=0.47-1.04). Thermally Stimulated Depolarization Currents (TSDC) as well as a single-point Kelvin probe (KP) System have been used in Metal-Insulator-Metal (MIM) capacitors, with the same charging conditions, in order to determine the total injected charge and the charge that was displaced through the bulk of each SiNx material. The experimental results revealed that the increase of Si-content results to an increase of dielectric charging but the injected charges are displaced faster through the bulk

material and towards the bottom electrode. Finally, the effective temperature is used in order to investigate hopping conduction that dominates charge transport in the bulk material and thus a more realistic approach of the discharging process is presented. return

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134 *Gate drive circuit for current balancing of parallel-connected SiC-JFETs under avalanche mode*

Taro Takamori (Tokyo Metropolitan University), Keiji Wada (Tokyo Metropolitan University), Wataru Saito (kyushu University) and Shin-ichi Nishizawa (kyushu University).

Abstract

This paper proposes a gate drive circuit for the current balancing of parallel-connected SiC-JFETs under avalanche mode. For a semiconductor DC circuit breaker, the power devices have to be connected in parallel to reduce the on-resistance and increase the limitation of current rating. In addition, it is reported that the SiC-JFET is suitable power devices from the view point of both conduction loss and degradation characteristics. This paper analyzes the behavior of current unbalance, and then designed the gate voltage and gate resistance in a gate drive circuit. The gate drive circuit can achieve the current balance equalization of parallel-connected SiC-JFETs under avalanche mode. The validity of the proposed gate drive circuit is verified by the experiment that uses 1.2~kV SiC-JFETs for a 400~V system. return

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135 *A Novel BIST for Monitoring Aging / Temperature by Self-Triggered Scheme to Improve the Reliability of STT-MRAM*

Yongliang Zhou (National ASIC System Engineering Center, Southeast University, Nanjing, 210096), Hao Cai (National ASIC System Engineering Center, Southeast University, Nanjing, 210096), Mengdi Zhang (National ASIC System Engineering Center, Southeast University, Nanjing, 210096), Lirida Naviner (Télécom Paris, 19 place Marguerite Perey Palaiseau, France, 91120) and Jun Yang (National ASIC System Engineering Center, Southeast University, Nanjing, 210096).

Abstract

This paper proposes a novel methodology to design high reliable STT-MRAM, with self-activated built-in-self-test (BIST) against aging/temperature-induced degradation. During sensing operation, Tunnelling magnetoresistance (TMR) is monitored, and real-time BIST is activated prior to permanent damage in Magnetic tunnel junction (MTJ) stack. To evaluate the feasibility of the test scheme, the proposed technique was involved in MRAM array implementation using 28-nm CMOS and 40-nm MTJ. HSPICE MOS Reliability Analysis (MOSRA) is used to evaluate the amount of electrical stress to the actual device aging degradation. Compared with previous periodical BIST method, the proposed self-triggered BIST saves ~31.1% cumulative power consumption over 12 years. And the proposed technique can improve reliability in the wear-out failure period. return

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136 *Faults and Reliability Analysis of Negative Resistance Converter Traction Power System*

Xiaofeng Yang (Beijing Jiaotong University), Jingda Gu (Beijing Jiaotong University), Trillion Q. Zheng (Beijing Jiaotong University) and Zhijun Zhao (Beijing Jiaotong University).

Abstract

To analyse the reliability of negative resistance converter traction power system (NRC-TPS), this paper discusses the short-circuit and open-circuit faults of its components. NRC-TPS is adopted to mitigate rail potential and stray current for the urban rail transit. The simulation results show that NRC-TPS can still mitigate rail potential and stray current at most faults. NRC-TPS is reliable for the urban rail transit to solve rail potential and stray current issues. return

137 *Analysis of the aging mechanism occurring at the bond-wire contact of IGBT power devices during power cycling*

Nausicaa Dornic (Université Gustave Eiffel), Ali Ibrahim (Université Gustave Eiffel), Zoubir Khatir (Université Gustave Eiffel), Nicolas Degrenne (Mitsubishi Electric R&D Centre Europe), Stefan Mollov (Mitsubishi Electric R&D Centre Europe) and Damien Ingrosso (Universite Gustave Eiffel).

Abstract

This paper focuses on the degradation at the wire bond contact with the metalized pad, and precisely its evolution with the power module aging. The goal is to highlight and understand the structural mechanisms occurring during the initiation and propagation of the cracks at the interface between the wire and metallization. In order to do so, accelerated power cycling tests with specific characterizations are carried out on special power modules. In addition, analysis of the interface wire-metallization are done with a numerical microscope and the EBSD (Electron Back-Scattered Diffraction) technique. As a result, an attempt to correlate the evolution of the degradation with that of the granular microstructure of the aluminium constituting the wire and metallization is proposed. *return*

138 *On the use of soft gamma radiation to characterize the pre-breakdown carrier multiplication in SiC power MOSFETs and its correlation to the TCR failure rate as measured by neutron irradiation*

Mauro Ciappa (ETH Zurich, Integrated Systems Laboratory) and Marco Pocaterra (ETH Zurich, Integrated Systems Laboratory).

Abstract

In this paper, some issues are solved that are encountered if using the high-energy gamma radiation for the non-invasive characterization of carrier multiplication in commercial, packaged SiC power devices under pre-breakdown conditions. For this scope the soft gamma emission of Am241 (59.9 keV) is exploited, which provides higher signal generation and a more efficient collimation of the sensing beam than in the Co60 and Cs137 radioactive gamma sources used in a previous work. Carrier multiplication factors are measured in two different SiC power MOSFETs under different bias conditions and compared to the values obtained from the high-energy sources. Literature failure rate data for single event burnout (terrestrial cosmic radiation) as measured by neutron irradiation are correlated to the multiplication factors as measured by the Am241 source. Finally, preliminary directions are issued to use of the multiplication factor as an indicator to define the bias derating factor for the devices under operation conditions. *return*

139 *On the replacement of water as coupling medium in scanning acoustic microscopy analysis of sensitive electronics components*

Michael Hertl (Predictive Image), Florie Mialhe (Centre Spatial de Toulouse) and Isaline Richard (Predictive Image).

Abstract

The present paper studies the use of isopropyl alcohol and fluorocarbon liquids as coupling fluids for acoustic microscopy non-destructive testing on electronic flight components, for which sometimes the standard coupling liquid water should be avoided in order to minimize sample contamination. The ultrasound velocities of three different fluorocarbon liquids are measured, and comparative failure analysis images on various electronics components are obtained by using five different coupling liquids. *return*

141 *Single-pulse observation of photoemission during avalanche breakdown in insulated gate bipolar transistor*

Koichi Endo (Toshiba Electronic Devices & Storage Corporation), Norimichi Chinone (Hamamatsu Photonics K.K.), Tomonori Nakamura (Hamamatsu Photonics K.K.), Toru Matsumoto (Hamamatsu Photonics K.K.) and Koji Nakamae (Osaka University).

Abstract

Photoemission associated with avalanche breakdown current of insulated gate bipolar transistor (IGBT) was observed using a multi-anode photomultiplier tube (PMT) with high time resolution of 20 ns. As PMT can detect very weak light, we could observe the photoemission even under applying a single pulse bias condition. The increase / decrease and movement of the light emission from the current filament were observed. It was also found that it changed every time the pulse was applied. *return*

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142 *CSME: A Novel Cycle-Sensing Margin Enhancement Scheme for High Yield STT-MRAM*

Mingyue Liu (National ASIC System Engineering Center, Southeast University, Nanjing, 210096), Hao Cai (National ASIC System Engineering Center, Southeast University, Nanjing, 210096), Yongliang Zhou (National ASIC System Engineering Center, Southeast University, Nanjing, 210096), Bo Liu (National ASIC System Engineering Center, Southeast University, Nanjing, 210096) and Lirida Naviner (Laboratoire Traitement et Communication de l'Information, Tel ´ ecom Paris, 91120 Palaiseau.).

Abstract

Spin-transfer torque (STT)-MRAM requires yield-aware design for hybrid magnetic-CMOS integration. In this paper, a novel cycle-sensing margin enhancement (CSME) scheme with pMOS assisted voltage-type sense amplifier (p-VSA) is proposed to alleviate imperfect process induced performance fluctuations. With iterated charging-discharging through non-volatile data path and reference path, read margin can be significantly improved thanks to enlarged sensing window. Simulation is performed using MTJ compact model and TSMC 28-nm process. Results show that ~14.1% read yield is realized at 50% tunnel magnetoresistance ratio (TMR), with 0.6V supply voltage comparing to conventional VSA. *return*

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143 *Heavy Ion and Proton Induced Single Event Upsets in 3D SRAM*

Ze He (Institute of modern physics, Chinese Academy of Sciences), Chang Cai (Institute of modern physics, Chinese Academy of Sciences), Tianqi Liu (Department of Computer Science and Technology, Tsinghua University), Bing Ye (Institute of Modern Physics, Chinese Academy of Sciences), Lihua Mo (Institute of Modern Physics, Chinese Academy of Sciences) and Jie Liu (Institute of Modern Physics, Chinese Academy of Sciences).

Abstract

Heavy ion and proton are used to investigate the radiation sensitivity of advanced 3D memory. The ionization effect dominants the SEU cross sections in proton irradiation. The ultra-high energy heavy ion can induce higher SEU cross sections than the ions with medium energy and barely enough range. Moreover, the ultra-high energy heavy ions are suitable to be used in evaluating the radiation sensitivity of 3D SRAM with intact packages, if the actual LET values are calculated effectively. *return*

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144 *Wear-out Failure of an IGBT Module in Motor Drives due to Uneven Thermal Impedance of Power Semiconductor Devices*

Ionut Vernica (Aalborg University), Ui-Min Choi (Seoul National University of Science and Technology), Huai Wang (Aalborg University) and Frede Blaabjerg (Aalborg University).

Abstract

In this paper, the uncertainties introduced by the variation of IGBT thermal impedance on the lifetime prediction of a motor drive IGBT module are investigated and quantified. A mission-profile-based reliability assessment procedure is first used to determine the reliability metrics of each IGBT in the inverter,

according to its individual thermal impedance characteristic. Afterwards, the impact of thermal impedance on the power module reliability evaluation is quantified, and three study-case scenarios are analysed. The uncertainty analysis has shown that a significant deviation is expected in the lifetime prediction of motor drive IGBT modules, if the thermal impedance of each individual transistor is not carefully considered during the analysis. *return*

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145 *Non Thermally-Activated Transients and Buffer Traps in GaN Transistors With p-Type Gate: a New Method for Extracting the Activation Energy*

Arianna Nardo (Università degli Studi di Padova), Meneghini (Università degli Studi di Padova), Barbato (Università degli Studi di Padova), De Santi (Università degli Studi di Padova), Meneghesso (Università degli Studi di Padova), Zanoni (Università degli Studi di Padova), Sicre (Infineon Technologies Austria AG), Sayadi (Infineon Technologies Austria AG), Prechtl (Infineon Technologies Austria AG) and Curatola (Infineon Technologies Austria AG).

Abstract

This paper demonstrates that conventional drain current transient (DCT) measurements fail at identifying the correct activation energy of buffer defects in transistors with p-GaN gate. Based on combined pulsed and transient characterization, we demonstrate that (i) under off-state stress, the analysed devices suffer from moderate dynamic-Ron and from positive shift in the threshold voltage; (ii) the de-trapping kinetics, analysed by DCT, are unexpectedly not thermally-activated; (iii) de-trapping kinetics are significantly accelerated when measured at high gate voltage; (iv) we report a power law correlation between the gate leakage measured during the de-trapping phase and the time constant for recovery. Finally, (v) we propose a new characterization procedure, based on TLM structures, to overcome these issues that prevent accurate characterization of buffer-related effects. *return*

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147 *Effects of Solder Degradation on the Die Temperature Measurement via Internal Gate Resistance*

Chihiro Kawahara (Mitsubishi Electric Corporation), Julio Brandelero (Mitsubishi Electric R&D Centre Europe), Stefan Mollov (Mitsubishi Electric R&D Centre Europe) and Pierre-Yves Pichon (Mitsubishi Electric R&D Centre Europe).

Abstract

Virtual junction temperature measurement via internal gate resistance(Tvg) is attractive for the health monitoring of the power modules. Using the gate resistance as TSEP permits precise and timely absolute temperature on the die where the gate is located. This paper investigates how this measurement relates to other parts of the power die, inclusive of ageing effects such as die attach degradation. A model has been developed to describe the temperature distribution, validated through FEM simulations and experimental measurements. *return*

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148 *A Novel On-Wafer Approach to Test the Stability of GaN-based Devices in Hard Switching Conditions: Study of Hot-Electron Effects*

Nicola Modolo (Università degli studi di Padova - DEI), Matteo Meneghini (Università degli studi di Padova - DEI), Alessandro Barbato (Università degli studi di Padova - DEI), Arianna Nardo (Università degli studi di Padova - DEI), Carlo De Santi (Università degli studi di Padova - DEI), Gaudenzio Meneghesso (Università degli studi di Padova - DEI), Enrico Zanoni (Università degli studi di Padova - DEI), Sebastien Sicre (Infineon Technologies Austria), Gerhard Prechtl (Infineon Technologies Austria) and Gilberto Curatola (Infineon Technologies Austria).

Abstract

In this work, a novel system to investigate the stability of GaN-based HEMT devices is presented, and used to investigate hot-electron effects. The developed system is used to study the impact of hard switching on

the dynamic on-resistance of such devices. In particular, we were able to obtain (on wafer level) a very fast turn-ON commutation with dV/dt>10 V/ns (representative of realistic conditions) thanks to the low parasitic at the drain node. As a result, a realistic performance assessment of the dynamic stress of GaN power HEMTs in now available at wafer level, thus shortening the technology development loop. By intentionally tuning the capacitance at the drain node we can accurately control the amount of energy/charge released during each hard switching event, thus being able to evaluate the impact of increasing stress conditions on the devices. The results indicate that even if the hard-switching lasts few nanoseconds, it significantly impacts the dynamic R_DSON: we conclude that hot-electron trapping can occur in ns-time scale.

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149 *Thermal Behaviour Evolution of an IGBT Chip After Aging Measured by Thermoreflectance*

Metayrek Youssef (SATIE lab,Gustave Eiffel University), Kociniewski Thierry (Groupe l'Etude de la Matière Condensée (CNRS and University of Versailles St Quentin)) and Khatir Zoubir (SATIE lab,Gustave Eiffel University).

Abstract

In this paper, we propose to study the thermal mapping evolution of the Insulated gate bipolar transistor (IGBT) emitter metallization after aging by thermoreflectance. Thermoreflectance measurements were done in static regime before and after aging by DC power cycling. The aim of this study is to observe the change in thermal behaviour at the cell level due to power cycling aging. Preliminary results indicate that pixel-by-pixel calibration eliminates artefact in reflectivity images and should allow a thermal calibration independently of the topography and chemical change of the metallization after cycling. *return*

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151 *Mission profile-oriented configuration of PV panels for lifetime and cost-efficiency of PV inverters*

Dingyi Wang (Hefei University of Technology, SUNGROW POWER SUPPLY Co., Ltd.), Haoran Wang (SUNGROW POWER SUPPLY Co., Ltd.) and Xing Zhang (Hefei University of Technology).

Abstract

In this paper, a comprehensive analysis, considering the real-field mission profile and influence from PV panel configuration is provided. The results show that with the increase of number of PV strings from 160 to 200 in an 800MW inverter, the daily average full-power duration could also increase from less than 1 hour to almost 3 hours, that making better cost-efficiency. While the lifetime of inverter, which is characterized by IGBT operation lifetime, decreases from 40 years to 20 years. *return*

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154 *Gold Wire Bond Study for Automotive Application*

Charalampos Papadopoulos (u-blox), Marta Cammarata (u-blox), Jan Prinz (u-blox), Consolato Morabito (u-blox), Thomas Villiger (u-blox), Sebastian Steiner (u-blox), Andy Rodriguez (Amkor Technology), Jaedoo Kwon (Amkor Technology), Joerg Krinke (Robert Bosch GmbH), Juergen Urban (Robert Bosch GmbH), Heidrun Kabus (Robert Bosch GmbH), Rolf Geilenkäuser (GLOBALFOUNDRIES Dresden Module One LLC & Co. KG), Jens Dienelt (GLOBALFOUNDRIES Dresden Module One LLC & Co. KG), Dirk Breuer (GLOBALFOUNDRIES Dresden Module One LLC & Co. KG) and Frank Kuechenmeister (GLOBALFOUNDRIES Dresden Module One LLC & Co. KG).

Abstract

In this publication, the influence of wire material properties (2N/4N) and plasma pre-treatment on the wire-bond strength is investigated, comparing the wire pull force capability and analysing the cross sections of the Au/Al bonds after High Temperature Storage Life (HTSL, 150°C), Temperature Cycling (TC, -65°C – 150 °C) and unbiased Humidity Accelerated Stress Test (uHAST, 130°C/85%RH). Furthermore, it will be shown how learning cycles can be accelerated by using elevated test temperatures (HTSL, 250°C). The effect of plasma treatment on 2N and 4N wires will also be discussed. Major impact factors on wire-bonding

reliability are bond pad thickness, pad opening and the corresponding Aluminium splash in dependence on the bond parameters settings with and without plasma treatment prior to wire bonding. return

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155 *Circuit Design using Schmitt Trigger to Reliability Improvement*

Alexandra Lackmann Zimpeck (Universidade Católica de Pelotas (UCPel)), Cristina Meinhardt (UFSC), Laurent Artola (ONERA/DPHY), Guillaume Hubert (ONERA/DPHY), Fernanda Kastensmidt (Universidade Federal do Rio Grande do Sul - UFRGS) and Ricardo Reis (UFRGS).

Abstract

This paper presents a design strategy to reduce the impact of process variations and soft error susceptibility in FinFET circuits. The mitigation is provided by connecting a Schmitt Trigger in the gate output. The improvements in power and delay variability can reach up to 32.6% and 42.1%, respectively, with logic cells almost immune to soft error even at the near-threshold regime. When compared with other circuit-level approaches such as sleep transistor, decoupling cells, and transistor reordering, on average, the Schmitt Trigger technique is at least 6%, 8%, and 10.5% more robust to process variability, respectively. return

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156 *Experimental results on gated diodes and BIMOS ESD devices in 28nm FD-SOI under TLP & TID radiation*

Philippe Galy (STMicroelectronics), Frederic Soto (STMicroelectronics), Johan Bourgeat (STMicroelectronics), Blaise Jacquier (STMicroelectronics), Valeria Kilchytska (ICTEAM / ELEN - UcL) and Denis Flandre (ICTEAM / ELEN - UcL).

Abstract

The electrostatic discharge (ESD) protection is a major concern for advanced CMOS technology manufacturing.Several solutions are available on market with efficient robustness and compliant with the ESD window especially in 28 nm FD-SOI technology. In the framework of harsh environment applications and to explore the performance under total ionizing dose (TID) radiation, it is important to investigate ESD protection devices such as gated and STI diodes in hybrid bulk or BIMOS solution in thin silicon film. This study is based on transmission line pulse (TLP)characterization before and after Co60 TID radiation in the range of [25 krad – 200 krad]. Following this analysis, we expect to gain better understanding of robustness and push the final performance of the device. The preliminaryresults will be useful to give a trend and to improve the device robustness against ESD and TID events and lead to more competitive solutions. return

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157 *Interface characterization of Cu-Cu ball bonds by a fast shear fatigue method*

Bernhard Czerny (CD Laboratory for Lifetime and Reliability of Interfaces in Complex Multi-Material Electronics, CTA, TU Wien) and Golta Khatibi (CD Laboratory for Lifetime and Reliability of Interfaces in Complex Multi-Material Electronics, CTA, TU Wien).

Abstract

A highly accelerated shear fatigue testing method is presented to test the long-term reliability and reveal the bonded interface of thermosonic Cu-Cu ball bonds. The method is an adaptation to a new industrial fatigue tester (BAMFIT) and can be conducted without an intricate specimen preparation. This method induces one-directional mechanical cyclic shear stresses to the Cu nailhead in order to initiate fatigue fracture until lift-off, revealing the actual bonded interface. This study compares the fatigue resistance of Cu wire to coarse and fine grained Cu and Al metallization. The fatigue results are accompanied by nano indentation tests and shear tests. The fatigue results showed the best performance for those bonded on coarse grained Cu pads (metallization), slightly less for fine grained Cu and at least a decade more than Cu-Al. Annealing the specimens prior to testing resulted in a slightly increases in Nf for Cu bonds on fine grained pads as well as for Cu-Al bonds. The Nf for coarse grained Cu pads remains the same but the scattering of the fatigue results increases. With the ability to compare the fatigue behaviour of the bonded interface within minutes, this method is most suitable for rapid qualification at an early stage of development. return

158 *Influence of copper and CdTe thickness in the reliability of CdS/CdTe solar cells*

Matteo Bertoncello (University of Padova), Fabio Casulli (University of Padova), Marco Barbato (University of Padova), Elisa Artegiani (University of Verona), Alessandro Romeo (University of Verona), Nicola Trivellin (Universiti of Padova), Enrico Zanoni (University of Padova), Matteo Meneghini (University of Padova) and Gaudenzio Meneghesso (University of Padova).

Abstract

The goal of this paper is to investigate the stability of CdTe solar cells exposed to high temperature storage. Several cells, having different thickness of copper in the contacts and of CdTe absorber were investigated. The results, obtained through combined EQE, dark and light IV, and photovoltage decay, indicate that the Cu metal contact plays a role in the degradation of the solar cells, and provide detailed insight on the related processes.
return

159 *Analysis of cyclic spontaneous switchings in GaN & SiC cascodes by snappy turn-off currents*

Yasin Gunaydin (University of Bristol), Saeed Jahdi (University of Bristol), Olayiwola Alatise (University of Warwick), Jose Ortiz Gonzalez (University of Warwick), Avinash Aithal (EA Technology), Xibo Yuan (University of Bristol) and Phil Mellor (University of Bristol).

Abstract

This paper investigates the crosstalk-induced spontaneous switchings and gate bouncing as continuous cycles of turn-on and turn-off transients as a key reliability bottleneck in SiC and GaN cascode power devices. The paper will present a wide range of measurements to describe the severity of unwanted switching cycles in presence of snappy turn-off current off a free-wheeling diode which results in a negative gate voltage induced by the source inductance of the cascode packaged devices. This is shown to lead to positive feedback loop, thermal runaway and eventual failure. Modelling is performed which confirms the theory described to explain the root cause of the continued oscillatory transients and comparisons are made with standalone SiC power MOSFETs. *return*

160 *An error detecting scheme with input offset regulation for Enhancing Reliability of ultralow-voltage SRAM*

Pan Yang (Anhui Institutes for Food and Drug control, Hefei, 230051), Xiaocan Ye (Anhui Institutes for Food and Drug control, Hefei, 230051), Yongxin Zhao (Anhui Institutes for Food and Drug control, Hefei, 230051), Wei Zhang (Anhui Institutes for Food and Drug control, Hefei, 230051), Shoumou Huang (Anhui Institutes for Food and Drug control, Hefei, 230051), Yang Huang (Anhui Institutes for Food and Drug control, Hefei, 230051) and Yujie Wang (Anhui Institutes for Food and Drug control, Hefei, 230051).

Abstract

This paper proposes a new scheme to improve the reliability and throughput of ultralow-voltage static random access memory (SRAM). The proposed scheme utilizes an error detecting sense amplifier (ED-SA) to constraint SRAM access timing, which combines timing error detection and correction. ED-SA applies different threshold transistors into the input terminals and regulates input offsets (Voffset) to the different polarity. By this way, the swing of BLs will be enhanced by one of the input offsets and its output will judge the other's correctness. Simulation results in TSMC 28nm CMOS process design kits show that the proposed scheme has a better reliability and achieves 2.49x throughput improvement compared with conventional ultralow voltage SRAMs. *return*

163 *Using of Bond-Wire Resistance as Ageing Indicator of Semiconductor Power Modules*

Ali Ibrahim (University Gustave Eiffel), Zoubir Khatir (University Gustave Eiffel), Jean-Pierre Ousten (University Gustave Eiffel), Richard Lallemand (University Gustave Eiffel), Nicolas Degrenne (Mitsubishi Electric R&D Centre Europe), Stefan Mollov (Mitsubishi Electric R&D Centre Europe) and Damien Ingrosso (Gustave Eiffel University).

Abstract

This paper studies the use of wire—bonds contact resistance as indicator to diagnose the health state of power electronics modules. This technique is especially dedicated to monitoring the degradation of the topside interconnection (metallization-wire bonds) when the module is wired with a Kelvin point. The main advantage of this indicator is that it can be followed online, without being disturbed by current or voltage, to diagnose the health state of the power module and, possibly, the prognosis of the remaining lifetime of the power module by associating it with a lifetime model. For this purpose, based on power-cycling tests in different conditions, a comparison between this indicator and the one commonly used, i.e. the collector-emitter voltage Vce, show that the first one is much more sensitive to the degradations, easier to use online and finally should be more suitable for lifetime prognosis. *return*

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164 *Mode Identification for Reliability Improvement of MMC*

Xiaofu Fan (South China University of Technology), Dongyuan Qiu (South China University of Technology), Bo Zhang (South China University of Technology), Yanfeng Chen (South China University of Technology), Runhong Huang (Electric Power Research Institute, China Southern Power Grid Co., Ltd), Wanyu Cao (Electric Power Research Institute, China Southern Power Grid Co., Ltd), Shukai Xu (Electric Power Research Institute, China Southern Power Grid Co., Ltd), Chuang Fu (Electric Power Research Institute, China Southern Power Grid Co., Ltd), Hong Rao (Electric Power Research Institute, China Southern Power Grid Co., Ltd) and Licheng Li (Electric Power Research Institute, China Southern Power Grid Co., Ltd).

Abstract

In order to improve the reliability of Modular Multilevel Converters (MMC), the unexpected modes which will lead to unintended outcomes should be identified. In this paper, the unexpected modes of semi-full-bridge (SFB) submodule are detected through superposition of passive components on different switching states according to the operation principles. Then, further analysis on triggered conditions and effect of unexpected modes is helpful to avoid potential threat on MMC, which is also an effective way to protect the normal operation of MMC. *return*

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166 *FEM-Aided Damage Model Calibration Method For Experimental Results*

Martin B. Fogsgaard (Aalborg University) and Francesco Iannuzzo (Aalborg University).

Abstract

This paper presents a novel loading evaluation procedure to be used for IGBT power cycling. The method is a combination of experimental life tests and finite element analysis digital twin. It was validated and predicted the life-time with 2.77% error, compared to the 8.78% error of the reference. *return*

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167 *Smart Soiling Sensor for PV Modules*

Marco Simonazzi (University of Parma), Giovanni Chiorboli (University of Parma), Paolo Cova (University of Parma), Roberto Menozzi (University of Parma), Danilo Santoro (University of Parma), Sergio Sapienza (University of Parma), Corrado Sciancalepore (University of Parma), Giovanna Sozzi (University of Parma) and Nicola Delmonte (University of Parma).

Abstract

In this work we propose a new sensor concept to evaluate the degradation of PV arrays due to soiling. It is based on the I-V curve analysis coupled with an artificial vision inspection of a reference PV module to

quantify and identify the type of dirt. Considering the use of this approach in the automatic scheduling of maintenance interventions in smartgrids, we developed a Simulink model of a DC nanogrid to test different control strategies. Here, early results are shown to demonstrate the effective-ness of the sensor. *return*

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168 *Reliability-Oriented Optimization of Aluminum Electrolytic Capacitor Considering Uncertain Mission Profile*

Hao Niu (Harbin Institute of Technology), Shujuan Wang (Harbin Institute of Technology) and Xuerong Ye (Harbin Institute of Technology).

Abstract

This paper proposes a reliability-oriented optimization method for aluminum electrolytic capacitors (Al-Caps) in a LED driver, which considers the uncertainty of operating conditions. The uncertainties of ambient temperature are modelled by kernel density estimation according to historical weather data. Then, the temperature stress of Al-Cap under operating condition is obtained by thermal simulation, and then the B10 lifetime of Al-Cap under uncertainties of mission profile is analysed by Monte Carlo simulation. Afterwards, the reliability optimization formulation is established by integrating the average and standard deviation of mission profile-based lifetime. Finally, the particle swarm algorithm is applied to solve the optimization problem for an optimal design of Al-Cap.

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169 *Packaging Reliability Estimation of High-Power Device Modules by Utilizing Silver Sintering Technology*

Chang-Chun Lee (Department of Power Mechanical Engineering, National Tsing Hua University), Kuo-Shu Kuo (Industrial Technology Research Institute), Chi-Wei Wang (Department of Power Mechanical Engineering, National Tsing Hua University), Jing-Yao Chang (Industrial Technology Research Institute), Wei-Kuo Han (Industrial Technology Research Institute) and Tao-Chih Chang (Industrial Technology Research Institute).

Abstract

In this study, a high-power device packaging composed of 600V/450A insulated gate bipolar transistor module is presented. To improve the thermal dissipation and decrease the junction temperature, the Ag paste sintering approach is applied instead of the conventional soldering processes. After conducting a thermal cycling test of up to 2000 cycles, the die shear strength of the sintered Ag is as high as 24.8 MPa. Lowering the induced stress to fracture failure is carefully suggested using finite element simulation. Furthermore, a reduction of –22% in the thermal resistance is measured. This research demonstrates that the application of the Ag paste sintering method in the 600V/450A insulated gate bipolar transistor module is dramatically useful. *return*

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170 *Analysis of trap states in AlGaN/GaN self-switching diodes via impedance measurements*

Elsa Pérez-Martín (Applied Physics Department, Salamanca University), Daniel Vaquero (NanoLab Usal, University of Salamanca), Hector Sánchez-Martín (Applied Physics Department, Salamanca University), Christophe Gaquière (Institut d'Electronique, de Microelectronique et de Nanotecnologie, University of Lille), Victor Javier Raposo (Applied Physics Department, Salamanca University), Tomás González (Applied Physics Department, Salamanca University), Javier Mateos (Applied Physics Department, Salamanca University) and Ignacio Iñiguez-de-la-Torre (Applied Physics Department, Salamanca University).

Abstract

In this contribution, the presence of trap states in self-switching diodes based on AlGaN/GaN has been identified by means of an AC characterization between 75 kHz to 30 MHz in a wide temperature range, from 70 K to 300 K. Measurements allow us to determine two different characteristic energies of the traps, 12

meV and 61 meV. The impact of the trapping effects on microwave detection at zero-bias has been analyzed in the same temperature range, the measured responsivity showing an unusual enhancement and a frequency roll-off at low temperatures. *return*

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171 *A Single-Trap Study of PBTI in SiON nMOS Transistors*

Michael Waltl (Institute for Microelectronics, TU Wien, Austria), Bernhard Stampfer (Institute for Microelectronics, TU Wien, Austria), Gerhard Rzepa (Global TCAD Solutions, Vienna, Austria), Ben Kaczer (imec, Leuven, Belgium) and Tibor Grasser (Institute for Microelectronics, TU Wien, Austria).

Abstract

To accurately study positive bias temperature instability (PBTI) in nanoscale SiON nMOS transistors we make use of the time-dependent defect spectroscopy (TDDS) and examine the device performance degradation at the single-defect level. Contrary to what is visible in large-area devices, our investigations clearly reveal charge trapping at both electron and hole traps contribute to the overall drift of the threshold voltage in these devices. Even though only electron trapping is typically considered for PBTI we observe that hole traps account foraround 20% of the total threshold voltage drift. To evaluate the impact of single-defects on the device performance we characterize the charge trapping kinetics of a number of defects, which can be explained employing a two-state defect model. In our approach we consider charge trapping due to defect/channel interaction for electron traps and defect/gate interaction for hole traps. From the extracted trap levels and trap depths we conclude that hole traps reside in the middle of the insulator while electron traps are located closer to the SiON/Si interface. Finally, the extracted trap parameters are fully consistent with defect candidates from DFT calculations. to be defined. *return*

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172 *A lifetime assessment and prediction method for large area solder joints*

Agnieszka Betzwar (TU Wien), Martin Lederer (TU Wien) and Golta Khatibi (TU Wien).

Abstract

Mechanical bending fatigue experiments were conducted on large area Pb-rich and SnSb-based model solder joints consisting of Cu-strip/solder/DCB substrates. Experimental lifetime curves in the range between 105 and 108 loading cycles at room and elevated temperature showed an improved fatigue resistance for SnSb alloys. Crack length as a function of loading cycles (da/dN) was determined for selected samples to study the cyclic degradation behaviour of the solder layer. Crack initiation and propagation in the joints was modelled on the basis of a damage accumulation rule considering the strain rate and temperature dependency of the solder alloy. Application of the FEM model to large area solder joints allowed calculation of the incremental advancement of the crack front, determination of the crack growth rate (da/dN) and prediction of lifetime under a given loading condition. *return*

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173 *A Method to Extract Lumped Thermal Networks of Capacitors for Reliability Oriented Design*

Nicola Delmonte (University of Parma), David Cabezuelo (University of the Basque Country), Iñigo Kortabarria (University of the Basque Country), Danilo Santoro (University of Parma), Andrea Toscani (University of Parma) and Paolo Cova (University of Parma).

Abstract

In this work we propose a procedure based on finite elements simulations to compute a lumped-parameter thermal model of capacitors. The extracted Foster, or Cauer network coupled to the electrical model can be useful to evaluate the temperature of capacitors in SPICE-like simulations. In this way, it is possible to evaluate the expected maximum operative temperature of the capacitor embedded in a circuit before its real application, avoiding unexpected failures since the prototyping stage. Here, we describe the workflow of the method and, finally, the proposed approach will be used for the design of snubber capacitors to be used in a medium power (60 kW) high frequency AC/AC converter. *return*

174 *UIS performance and ruggedness of stand-alone and cascode SiC JFETs*

Sunday Nereus Agbo (The University of Warwick), Jose Ortiz Gonzalez (The University of Warwick), Ruizhu Wu (University of Warwick), Saeed Jahdi (University of Bristol) and Olayiwola Alatise (The University of Warwick).

Abstract

In this paper the ruggedness of stand-alone and cascode SiC JFETs is evaluated under single and repetitive unclamped inductive switching (UIS). The impact of the JFET gate resistance, avalanche current and temperature are evaluated. The results show that the avalanche characteristics are strongly affected by the peak avalanche current and the JFET gate resistance, due to the significant gate leakage current that results from impact ionisation. This gate leakage current plays a fundamental role on the reduced performance under repetitive UIS of cascode SiC JFETs compared with stand-alone SiC JFETs. *return*

176 *Extraction of Wearout Model Parameters using On-Line Test of an SRAM*

Shu-Han Hsu (Georgia Tech Institute of Technology), Ying-Yuan Huang (Georgia Tech Institute of Technology), Yi-da Wu (Georgia Tech Institute of Technology), Kexin Yang (Georgia Tech Institute of Technology), Li-Hsiang Lin (Georgia Institute of Technology) and Linda Milor (Georgia Institute of Technology).

Abstract

To accurately determine the reliability of SRAMs, we propose a method to estimate the wearout parameters of FEOL TDDB using on-line data collected during operations. Errors in estimating lifetime model parameters are determined as a function of time, which are based on the available failure sample size. Systematic errors are also computed due to uncertainty in estimation of temperature and supply voltage during operations, as well as uncertainty in process parameters. *return*

177 *Reliable Endpoint Technique on Si trenching for Backside Circuit Edit*

Hideo Tanaka (Thermo Fisher Scientific) and Chun-Cheng Tsao (Thermo Fisher Scientfic).

Abstract

Circuit Edit (CE) techniques have been used for debug, characterization and prototyping, etc. in the IC industry. CE jobs have become more complex to accomplish since the adaption of FinFET technology. Backside Si trenching in part of CE process is required to have the highest success rate because once punched through Si trench floor, the IC would lose functionality. Therefore, it needs reliable and quantitative end-pointing technique. The coaxial FIB column technology [1] allows to obtain optical image simultaneously, so optical interference fringes can be sued to estimate remaining of Si thickness, to monitor planarity of trench floor and to obtain trenching end-point. We introduce reliable end-pointing technique on backside Si trenching. *return*

178 *FPGA-based reliability testing and analysis for 3D NAND flash memory*

Debao Wei (Harbin Institute of Technology), Zhelong Piao (Harbin Institute of Technology), Hua Feng (Harbin Institute of Technology), Liyan Qiao (Harbin Institute of Technology) and Xiyuan Peng (Harbin Institute of Technology).

Abstract

NAND flash memory is widely employed for its inherent advantages, such as high storage density, high reliability, low power consumption, and shock resistance. 3D NAND flash technology brings some new reliability challenges due to the inter-layer differences caused by the stacking process. The reliability community has made significant efforts to study flash memory management algorithms to reduce the reliability loss of storage media. In view of this, it is essential to develop an efficient and accurate experimental platform for NAND flash memory management algorithms. In order to obtain the complete

endurance test data of the flash memory chip and study the change of the relevant physical quantities in the lifetime cycle of the flash memory, this research designs a experimental platform that supports multiple packages and various types of NAND flash memory chips, conducts reliability index collection, and studies a newly discovered reliability problem of 3D NAND Flash memory. We obtain the original test data from our experimental platform for 3D NAND flash memory. Figure 1 shows a photograph of our 3D NAND flash experimental platform. The FPGA controller model used in this hardware platform is EP4CE15E22C8, which is an Altera FPGA. The selected NAND flash memory chip is MT29F64G08CBCGB, which is a 3D MLC NAND flash from Micron Inc. E2PROM is utilized to record experimental information. 100M Ethernet interface is used to communicate between the hardware platform and the host. The host interactive interface is built on LabVIEW. We find that performing continuous read operations on an idle 3D NAND flash does not get a stable number of error bits, which show a clear difference from the situation of 2D NAND flash. There will be a significant decrease in the number of error bits retrieved after the first read, and then it will gradually stabilize (as shown in Fig. 2). Therefore, it is inappropriate to consider that the data obtained by performing only one read operation is valid. We study the characteristics and countermeasures of this phenomenon from the following three aspects. First, we find that the drop in the number of error bits occurred a few seconds after the first read operation. After performing the first read on an idle flash and wait for 0, 10, 30, and 60 seconds, we find that the number of error bits requires fewer reads to stabilize (as shown in Fig. 3). In view of this, the measures we have taken to deal with this phenomenon are to perform the first read operation and wait for a few seconds before thinking that the read data is reliable, or perform enough reads operation until the number of error bits obtained is stable. Second, if continuous block reads are performed immediately after the program operation, the read data will be unstable (as shown in Fig. 4).The number of error bits is also lower than that retrieved when the read data is stable. It takes a few minutes for reading data to be stable. In addition, a significant decrease in the number of error bits is also reported after the first read even in this case. Third, to study the effect of P/E cycles on this phenomenon,we obtain 40 sets of Raw Bit Error Rate (RBER) from continuous block reads after different P/E cycles, ranging from 100 to 10,000 (as shown in Fig.5). We find that within all the lifetime of the flash memory this phenomenon exists, and more P/E cycles leads to longer time for the data to stabilize after the first read. Through the above, we also measure the endurance of the chip. The relationship between the RBER and P/E cycles is given in Figure 6. The RBER range is from the level of 10-5 to 10-4. The reliable endurance limit is 10,000 P/E cycles, which is 5 times the endurance mentioned in the chip datasheet. In addition, there is a significant increase in RBER at the end of chip lifetime. Figure 7 shows the distribution of the number of error bits per page of an ordinary block after P/E cycles operation. The shaded area in the figure indicates the number of error bits of the block. 16 pages at each end are SLC pages, which have fewer error bits. The error bits are mainly distributed on the shared pages, and more error bits are concentrated at both ends of shared pages. We also test the effect of P/E cycles on the standard deviation of error bits on per page (as shown in Fig. 8). There are nine sets of data, varying from 100 to 8000 P/E cycles. It can be observed that with the increase of the of P/E cycles, the standard deviation of error bits on per page also increases. There is also a significant dispersion standard increase at the end of the chip lifetime. *return*

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181 *Single-event induced failure mode of PWM in DC/DC converter*

Jiantou Gao (Institute of Microelectronics, Chinese Academy of Sciences), Cai Li (Innovation Academy for Microsatellites, Chinese Academy of Sciences), Binhong Li (IMECAS), Bo Li (Institute of Microelectronics, Chinese Academy of Sciences), Fazhan Zhao (Institute of Microelectronics of Chinese Academy of Sciences), Jing Li (Institute of Microelectronics, Chinese Academy of Sciences), Gang Zhang (Institute of Microelectronics, Chinese Academy of Sciences), Chunlin Wang (Key Laboratory of Silicon Device Technology ,Institute of Microelectronics, Chinese Academy of Sciences), Chuanbin Zeng (Key Laboratory of Silicon Device Technology ,Institute of Microelectronics, Chinese Academy of Sciences), Jie Liu (Materials Research Centre, Institute of Modern Physics, Chinese Academy of Sciences), Shuai Cui (Innovation Academy for Microsatellites, Chinese Academy of Sciences), Qinzhi Wu (Innovation Academy for Microsatellites, Chinese Academy of Sciences) and Tianchun Ye (Institute of Microelectronics, Chinese Academy of Sciences).

Abstract

The single event effect (SEE) experiment towards a pulse width modulator (PWM) within the DC/DC converter was carried out by Ta+ ions (LET =83.53 MeV•cm2/mg) so as to reveal the single-event induced failure mechanisms. In order to figure out the perturbation and its propagation, an additional experiment of a standalone PWM illustrated two modes that possible address the operation failure in DC/DC converter

including the low-level output error and the high-level one. Matlab model reveals the relationship between the SEE in PWM and subsequent SET in DC/DC converter. return

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182 *FBGA solder ball defect effect on DDR4 data signal rise time and ISI measured by loading the data line with a capacitor*

Muhammad Waqar (Hanyang University), Sanghyeon Baeg (Hanyang University), Geunyong Bak (Hanyang University), Junhyeong Kwon (Hanyang University), Kiseok Lee (Hanyang University) and Sang Hoon Jeon (Hanyang University).

Abstract

This paper proposes a new method of investigating the effect of void or fracture in FBGA solder ball on the DDR4 data signal rise time and inter-symbol interference (ISI), by loading the data line with a capacitor. A void or fracture in solder ball increases its capacitance which effects the data signal rise time and increases ISI. For measuring ISI large patterns of 1's or 0's followed by a changing bit are used. However in in-field systems it is not possible to run large patterns of 1's or 0's. So the data line is loaded with a 0.2pF capacitive load on a UDIMM test card to mimic the increased capacitance due to FBGA solder ball void defect of height 0.2 mm and cross sectional area of 0.045 mm2. The loaded line shows increase in rise time of 16 ps. For loaded line the data eye opening is 0.077 UI lesser. This decrease in data eye means more ISI and it will cause increase in intermittent errors. return

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184 *Failure-analysis method of soldering interfaces in light-emitting diode packages based on time-domain transient thermal response*

Byongjin Ma (Korea Electronics Technology Institute).

Abstract

New soldering-interface failure-analysis method based on the transient thermal of the LED packages are proposed. This method is based on a physical property that the change of the junction temperature, which is monitored by voltage, represents the change of thermal gradient in the LED packages. Fast time-domain algorithm for failure-sensitivity enhancement was developed. And the feasibility of this algorithm was verified using a two-point measurement method during a thermal shock test. return

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187 *Influence of Temperature and Humidity on Power Cycling Capability of Power Modules*

Felix Wuest (Fraunhofer Institute for Reliability and Microintegration (IZM)), Olaf Wittler (Fraunhofer Institute for Reliability and Microintegration (IZM)) and Martin Schneider-Ramelow (Technische Universität Berlin).

Abstract

Since power electronics becomes more and more important for harsh environments, its power cycling capability under these conditions needs to be known. The goal of this research is to identify how high temperature and humid environments contribute to the damage of power modules during power cycling. Therefore, IGBT modules are tested with power cycling in cold environment, hot, dry environment and hot, humid environment. Additionally, High Humidity High Temperature Reverse Bias testing is done for comparison of different failure mechanisms. Power modules under warm, humid conditions fail significantly earlier than in warm, dry, or even cold, dry environment. This is mainly attributed to two effects. Firstly to the moisture swelling and thermal expansion of the housing material at higher temperatures and humidity which have an influence on the pressure on the thermal interface and secondly the moisture uptake capability of the thermal interface material. return

188 *Magnetic field imaging and light induced capacitance alteration for failure analysis of Cu-TSV interconnects*

Ingrid De Wolf (imec), Kristof J.P. Jacobs (imec) and Antonio Orozco (Neocera).

Abstract

This paper discusses Cu-filled Through Silicon Via (TSV) failure analysis cases where known FA methods were used in an alternative way. Results are shown using magnetic field imaging (MFI) on a cross-sectioned chip to detect a liner breakdown position, and MFI and Light Induced Capacitance Alteration (LICA) to detect opens in TSV daisy chains. *return*

189 *Impact of stray-inductance imbalance on short-circuit capability of multi-chip SiC power modules*

Kazuhiro Chou (University of Tsukuba), Takanori Isobe (University of Tsukuba) and Tomoyuki Mannen (University of Tsukuba).

Abstract

This paper discusses whether short-circuit capability of multi-chip SiC-MOSFET power modules is affected by stray-inductance imbalance between the chips. Experimental power modules equipped with commercial 1.2-kV, 19-A SiC-MOSFET chips are designed and fabricated in three different internal layouts, and then short-circuit capability of the power modules was measured. The experimental results show that the significant effect of stray-inductance imbalance can be seen only for 20 ns after the short-circuit event start. As a result, this paper reveals that multi-chip power module design doesn't need to pay attention to imbalance of stray inductance from the perspective of the short-circuit robustness. *return*

190 *Comparisons of SnO2 Gas Sensor Degradation under Elevated Storage and Working Conditions*

Yongquan Sun (Institute of Sensor and Reliability Engineering (ISRE);Harbin University of Science and Technology), Jiaying Guo (Institute of Sensor and Reliability Engineering (ISRE);Harbin University of Science and Technology), Jia Qi (Harbin University of Science and Technology), Bo Liu (Harbin University of Science and Technology) and Tianhua Yu (Harbin University of Science and Technology).

Abstract

Stability is an important performance indicator for SnO2 gas sensor and affected by temperature. Commercial SnO2 gas sensors are stored at environment temperature but operating at a temperature above 200 °C heated by a strip heater under a DC power supply. The degradation behaviors during storage were not identified and the differences of the degradation processes between storage and operation stages need to be further understood. This paper investigated degradation of SnO2 sensors under elevated environmental temperature and heating voltage conditions to interpret sensor instability. *return*

192 *Lithium-ion battery SoH estimation based on incremental capacity peak tracking at several current levels for online application*

Matthieu Maures (Univ. Bordeaux, CNRS, Bordeaux INP, IMS, UMR 5218), Armande Capitaine (Univ. Bordeaux, CNRS, Bordeaux INP, IMS, UMR 5218), Jean-Yves Delétage (Univ. Bordeaux, CNRS, Bordeaux INP, IMS, UMR 5218), Jean-Michel Vinassa (Univ. Bordeaux, CNRS, Bordeaux INP, IMS, UMR 5218) and Olivier Briat (Univ. Bordeaux, CNRS, Bordeaux INP, IMS, UMR 5218).

Abstract

In this paper, an extension to high C-rates of State of Health (SoH) diagnostic methods based on Incremental Capacity (IC) peak tracking is proposed. A set of eleven NCA Lithium-ion batteries who went

under different ageing protocol is used. Charge and discharge cycles are performed at C/20, C/10, C/5 and C/2, and then used for IC analysis. Correlations between the variations of IC peaks and SoH are presented and modelized, and shown to be accurate estimators for all tested C-rates.

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193 *Can automotive MEMS be reliably used in space applications? An assessment method under sequential bi-parameter testing*

Maxime Auchlin (CSEM SA), Ivan Marozau (CSEM SA), Dara Zaman Bayat (CSEM SA), Laurent Marchand (European Space Agency), Volker Gass (Ecole Polytechnique Fédérale de Lausanne (EPFL), Swiss Space Center (SSC)) and Olha Sereda (CSEM SA).

Abstract

Commercial Off-The-Shelf (COTS) automotive inertial measurement units were subjected to severe accumulative stress conditions: thermal shocks (high temperature gradients), temperature cycling (low gradients) and mechanical vibration are combined in an A-then-B sequential testing procedure, with the aim to promote failure acceleration and improve lifetime prediction. The maximum stresses, applied individually, did not cause failure on the selected components. On the other hand, accumulative bi-parameter testing conditions resulted in die attach delamination. Three batches of devices tested with different preconditioning (A-then-B or B-then-A) display different reliability figures. Failure mode and effects analysis (FMEA) is established. A Finite Element Analysis (FEA) is done based on a destructive physical analysis of the devices to confirm the correlation between the stresses applied and the physics of the failure in order to understand the thermomechanical behaviour of the devices, linking it to observed failures. *return*

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194 *A 3-D thermal network model for the temperature monitoring of thermal grease as interface material*

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(State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Xi'an, China).

Abstract

Abstract –In order to study the influence of thermal grease applied as thermal interface material between IGBT (insulated gate bipolar transistor) module and heat sink on the junction temperature of IGBT module under long term load profiles, a 3-D thermal network based on thermal grease temperature monitoring is proposed. Firstly, the finite element simulation model of IGBT module and heat sink containing thermal grease is established. Then, considering thermal coupling effect, the temperature distribution of thermal grease is obtained and the temperature monitoring points of thermal grease are determined in the finite element simulation. Finally, a 3-D thermal network is established to monitor the temperature in all regions of thermal grease. The temperature distribution of thermal grease under long term load profiles is obtained and the influence of thermal grease degradation on the junction temperature of IGBT module is analyzed. The proposed 3-D thermal network model based on the precise monitoring of thermal grease can increase the accuracy of IGBT module reliability analysis. *return*

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195 *Exploration of Gate Trench Module for Vertical GaN devices*

Maria Ruzzarin (University of Padova, Department of Information Engineering), Karen Geens (imec), Matteo Borga (imec), Hu Liang (imec), Shuzhen You (imec), Benoit Bakeroot (CMST, imec and Ghent University), Stefaan Decoutere (imec), Carlo De Santi (University of Padova, Department of Information Engineering), Andrea Neviani (University of Padova, Department of Infromation Engineering), Matteo Meneghini (University of Padova, Department of Information Engineering), Gaudenzio Meneghesso (University of Padova, Department of Information Engineering) and Enrico Zanoni (University of Padova, Department of Information Engineering).

Abstract

The aim of this work is to present the optimization of the gate trench module for use in vertical GaN devices in terms of cleaning process of the etched surface of the gate trench, thickness of gate dielectric and magnesium concentration of the p-GaN layer. On the basis of experimental results, we report that: (i) a good cleaning process of the etched GaN surface of the gate trench is a key factor to enhance the device performance, (ii) a gate dielectric >35-nm SiO2 results in a narrow distribution for DC characteristics, (iii) lowering the p-doping in the p-GaN layer decreases the ON-resistance (RON).

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196 *Barrier properties analysis of Cu/TiW/ITO electrode for Si heterojunction solar cell under thermal aging*

Jae-Seong Jeong (Korea Electron Technology Institute (KETI)).

Abstract

The front side metallization of silicon heterojunction (SHJ) solar cell was fabricated by electroless copper plating. The front electrode was composed of a copper/copper seed/TiW/ITO structure applied TiW layer as a diffusion barrier. In this paper, it was investigated the changes of TiW diffusion barrier under environmental stress. To analyze the barrier stability of TiW, samples for aging were fabricated by depositing copper seed/TiW/ITO on glass. The environment stress was applied to stress of the thermal aging (85ºC /1,000 hr). The stability of layer structure was analyzed by TiW thickness split (20nm, 50nm, 100nm) under environmental stress. Thermal oxidation on copper seed surface was depend on TiW thickness. The Cu2O phase was mainly formed with increase of TiW thickness. ITO diffused towards copper seed through TiW. *return*

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198 *Conducted EMI Susceptibility Analysis of a COTS Processor as Function of Aging*

Fabian Vargas (Catholic University - PUCRS), Juliano Benfica (Catholic University - PUCRS), Matheus Fay Soares (Catholic University - PUCRS) and Dorian Schramm (Catholic University - PUCRS).

Abstract

This work analyses the conducted electromagnetic immunity (EMI) of the Cortex-M4 processor as function of aging. Voltage dips were injected in the VDD input power pins of the processor as ruled by the IEC 61000-4-29 standard, whereas aging test was performed by means of the 1015.9 Burn-In Part of the Method MIL-STD-833E. We observed that after 456 hours at 125°C, the processor presented a current increase in excess of 2.36%, an average increase in the conducted EMI susceptibility in the order of 38% and negligible performance degradation according to the Dhrystone V2.1a benchmark. *return*

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199 *Shoot-through protection for an inverter consisting of the next-generation IGBTs with gate impedance reduction*

Kazunori Hasegawa (Kyushu Istitute of Technology), Seiya Abe (Kyushu Institute of Technology), Masanori Tsukuda (Green Electronics Research Institute, Kitakyushu), Ichiro Omura (Kyushu Institute of Technology) and Tamotsu Ninomiya (Green Electronics Research Institute, Kitakyushu).

Abstract

Attention has been paid to the next-generation IGBT toward CMOS compatible wafer processes, which can be driven by a 5-V logic level due to its low threshold gate voltage. This low threshold voltage makes the so-called shoot-through phenomena severer. This paper presents shoot-through protection for an inverter consisting of the next-generation IGBTs with gate impedance reduction, which reveals the criterion of the gate impedance with taking parasitic parameters of the inverter into account. *return*

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201 *Design Exploration of Majority Voter Architectures based on the Signal Probability for TMR Strategy Optimization in Space Applications*

Ygor Q. Aguiar (Université de Montpellier - IES/RADIAC), Frédéric Wrobel (IES), Jean-Luc Autran (Aix-Marseille University), Paul Leroux (University of Leuven - KU Leuven), Frédéric Sagné (IES), Vincent Pouget (IES - CNRS) and Antoine Touboul (UNIVERSITE DE MONTPELLIER II).

Abstract

An application-specific Single-Event Transient (SET) characterization based on the signal probability is proposed to optimize the Triple-Modular Redundancy (TMR) block insertion methodologies. Results show that the SET cross-section of complex-gate architectures presents low input dependence while for the NOR/NAND based architectures a higher dependence is observed due to logical masking effects. Additionally, different from the other architectures, the NAND voter has shown a reduction on the SET rate as the signal probability is increased. *return*

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202 *Hot-carrier-injection resilient RF power amplifier using adaptive bias*

Sebastián Matías Pazos (UIDI CONICET - UTN.BA), Fernando Leonel Aguirre (UIDI CONICET - UTN.BA), Félix Palumbo (UIDI CONICET - UTN.BA) and Fernando Silveira (IIE FING - UDELAR).

Abstract

An adaptive bias strategy is proposed to harden fully integrated CMOS RF power amplifiers against time-dependent parametric degradation due to hot carrier injection. PA transistor DC current is compared to a reference using an operational transconductance amplifier that provides an adaptive gate DC voltage to the PA transistor as its threshold voltage increases due to stress. Based on degradation modeling obtained from experimental accelerated aging of a transistor and a RF PA implemented on a 130 nm technology, time dependent simulation results of the adaptive bias show that the proposed circuit effectively compensates for the threshold voltage increase of the main transistor. *return*

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203 *On the Analysis of radiation-induced Failures in the AXI Interconnect Module*

Corrado De Sio (Politecnico di Torino), Sarah Azimi (Politecnico di Torino) and Luca Sterpone (Politecnico di Torino).

Abstract

In this paper, a fault injection campaign is performed in order to emulate the radiation-induced effects on the configuration memory of AP-SoC Zynq 7000, specifically targeting the interconnection module implemented on the programmable logic. This Interconnection Module is crucial for a wide range of applications and mitigation techniques such as hardware-accelerated designs, Dynamic Partial Reconfiguration or Triple Modular Redundancy, especially if they aim to meet high performance and high bandwidth. The fault injection results have been analyzed and classified accordingly with the effect observed on the processor-system side in terms of availability and fault model affecting data computed by the IP Cores implemented on the programable logic of the SoC. *return*

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204 *OFF-state Trapping Phenomena in GaN HEMTs: Interplay Between Gate Trapping, Acceptor Ionization and Positive Charge Redistribution*

Eleonora Canato (University of Padova), Matteo Meneghini (University of Padova), Carlo De Santi (University of Padova), Fabrizio Masin (University of Padova), Arno Stockman (ON Semiconductor), Peter Moens (ON Semiconductor), Enrico Zanoni (University of Padova) and Gaudenzio Meneghesso (University of Padova).

Abstract

We present an extensive analysis of the trapping processes induced by drain bias stress in AlGaN/GaN high-electron-mobility transistors (HEMTs) with p-GaN gate. We demonstrate that: (i) with increasing drain stress, pulsed I-V show an initial positive VTH variation and an increase in RON then, for drain voltages >100 V, VTH is stable and the RON shows a partial recovery. (ii) At moderate voltages, VTH instability is related to trapping at the gate stack, due residual negative charge left behind by the holes that leave the p-GaN layer through the Schottky gate contact and/or to trapping at the barrier. At higher voltages, we demonstrate the interplay of two trapping processes by C-V and pulsed drain current analysis: (iii) a fast storage of positive charge, accumulated in near the buffer/SRL interface, not strongly thermally activated, dominating at higher voltages; (iv) a slower negative charge storage, thermally activated. *return*

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206 *Degradation mechanisms in high power InGaN semiconductor lasers investigated by electrical, optical, spectral and C-DLTS measurements*

Francesco Piva (University of Padova - Department of Information Engineering), Carlo De Santi (University of Padova - Department of Information Engineering), Matteo Buffolo (University of Padova - Department of Information Engineering), Mattia Taffarel (University of Padova - Department of Information Engineering), Gaudenzio Meneghesso (University of Padova - Department of Information Engineering), Enrico Zanoni (University of Padova - Department of Information Engineering) and Matteo Meneghini (University of Padova - Department of Information Engineering).

Abstract

The aim of this work is to study the degradation processes in high power InGaN semiconductor lasers, by means of electrical, optical, spectral and capacitance deep-level transient spectroscopy measurements. The devices were submitted to two different stress experiments, (i) a constant current stress at 1.5 A at 45 °C, and (ii) a temperature/bias step stress at 1 A and increasing temperature. Results demonstrated: (i) two different mechanisms that change the drive voltage, one due to the activation of Mg and one ascribed to the generation of point defects; (ii) a parasitic peak is present in the emission spectra, ascribed to the recombination in a second quantum well (QW); (iii) redistribution of charge takes place during the temperature step stress. *return*

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207 *Evaluating the Soft Error Sensitivity of a GPU-based SoC for Matrix Multiplication*

German Leon (Universitat Jaume I de Castellon), Jose M. Badia (Universitat Jaume I de Castellon), Jose A. Belloch (Universidad Carlos III de Madrid), Almudena Lindoso (Universidad Carlos III de Madrid) and Luis Entrena (Universidad Carlos III de Madrid).

Abstract

System-on-Chip (SoC) devices can be composed of low-power multicore processors combined with a small graphics accelerator (or GPU) which offers a trade-off between computational capacity and low-power consumption. In this work we use the LLFI-GPU fault injection tool on one of these devices to compare the sensitivity to soft errors of two different CUDA versions of matrix multiplication benchmark. Specifically, we perform fault injection campaigns on a Jetson TK1 development kit, a board equipped with a SoC including an NVIDIA "Kepler" Graphics Processing Unit (GPU). We evaluate the effect of modifying the size of the problem and also the thread-block size on the behaviour of the algorithms. Our results show that the block version of the matrix multiplication benchmark that leverages the shared memory of the GPU is not only faster than the element-wise version, but it is also much more resilient to soft errors. We also use the cuda-gdb debugger to analyze the main causes of the crashes in the code due to soft errors. Our experiments show that most of the errors are due to accesses to invalid positions of the different memories of the GPU, which causes that the block version suffers a higher percentage of this kind of errors. *return*

208 *Accelerated aging test for gate oxide degradation in SiC MOSFETs for condition monitoring*

Shin-Ichiro Hayashi (Tokyo Metropolitan University) and Keiji Wada (Tokyo Metropolitan University).

Abstract

Herein, a method for condition monitoring of the gate oxide degradation for SiC MOSFETs is presented. To identify gate oxide degradation in SiC MOSFETs, a high-temperature gate bias (HTGB) test, which is an accelerated aging test, is usually performed. This paper proposes an advanced HTGB test. The test is suitable for developing a condition monitoring circuit because the test can accelerate the device aging under switching conditions. Using the test results, the parameter shifts of gate threshold voltage and gate capacitance are demonstrated, and condition monitoring technique is considered. *return215*

209 *A comparison study on electromagnetic susceptibility of current reference circuits with scaling-down technologies and schemes*

Zhian Wang (School of Microelectronics, University of Chinese Academy of Sciences, Beijing China), Binhong Li (Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China), Jianfei Wu (Tianjin Advanced Technology Research Institute, Tianjin, China), Wenxin Zhao (Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China), Bo Li (Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China), Hainan Liu (Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China), Chongjie Guan (School of Microelectronics, Beijing University of Technology, Beijing, China), Shiwei Feng (School of Microelectronics, Beijing University of Technology, Beijing, China), Jiajun Luo (Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China) and Tianchun Ye (Institute of Microelectronics of Chinese Academy of Sciences, Beijing, China).

Abstract

This paper studies the effects of feature sizes and circuit schemes on the electromagnetic susceptibility (EMS) of current reference circuits. Three reference circuits with PDSOI process sizes of 0.5μm (VREF50), 0.35μm (VREF33) and 0.18μm (VREF18) were used, and VREF50 has an additional CASCODE structure to achieve a PSRR enhancement. The test results showed that when the electromagnetic interference (EMI)is injected into the terminals VDD and VSS, the reference currents in both of the three circuits exhibited a negative shift. The main reason is that the drain voltage of the transistor close to the terminal VDD fluctuates greatly, causing a deviation from the saturation to the linear region from time to time, hence reducing the average value of the current. The higher voltage margin with the large process node, the stronger the immunity of the reference circuit to EMI. It is worth noting that the CASCODE structure has a negative effect on low frequency large-signal EMI. Therefore, VREF50 and VREF33 have the similar EMS. In a higher frequency range, the parasitic effect brought by the CASCODE structure becomes more serious, which increases the high-frequency impedance of the circuit. Finally, simulation results showed that the immunity level was improved by decreasing bypass capacitor between the sensitive node and the VDD to reduce the EMI injection, and replacing the nonlinear device by a positive temperature coefficient resistor to improve the circuit linearity. *return*

210 *Health monitoring of mechanically fatigued flexible lithium ion battery by electrochemical impedance spectroscopy*

Jae-Yeon Kim (Seoul National university of science and technology), Jin-Yeong Kim (Seoul National university of science and technology), Mu-Kyeong Kim (Seoul National university of science and technology) and Jai-Won Byeon (Seoul National university of science and technology).

Abstract

For reliable applications of flexible lithium ion batteries, the states of mechanically fatigued batteries were evaluated by applying electrochemical impedance spectroscopy (EIS). The EIS resistance of the batteries increased with mechanical fatigue, and this tendency was more distinct for the battery in the charged state. The EIS resistance of the fatigued battery was unstable and fluctuated during subsequent storage time after

fatigue. Capacity degradation of the fatigued battery was about three times faster than that of the as-received one. By scanning electron microscopic observation of the dissembled electrode materials, root causes of the observed faster degradations were attributed to lithium metal precipitation on the carbon negative electrode as well as collapse of lamellae structures of the polymer separator (i.e., blockage of micro pores for lithium ion movement.) *return*

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212 *Effect of integrated anneal optimizations of electroplated Cu thin films Interconnects*

Yasmin Abdul Wahab (University of Malaya), Mohd Rafie Johan (University of Malaya), Nor Aliya Hamizi (University of Malaya), Omid Akbarzadeh (University of Malaya), Zaira Zaman Chowdhury (University of Malaya) and Suresh Sagadevan (University of Malaya).

Abstract

The significance of this paper is to emphasize wafer scale electrochemical plating process optimizations to demonstrate yield-limiting defects reduction. A multiple process enhancement has been implemented to reduce metal “stress –induced” voids, crater defects, Cu mound, as well as other killer defects. The troubleshooting is involving thermal anneal conditions with the modifications of in-situ anneal to integrated helium anneal by demonstrating capability of ramp rates during heating and cooling stages. Result shows a significant defects reduction and reveals the dependence of anneal soak time particularly for types of defects. Due to this integration of concerns, we further investigate the adoption of integrated diffuser to quantify the best degree of uniformity and high resistivity to enhance an even current distribution on the wafer. The results show that uniformity of the deposited film has been improved significantly with an increasing trend with anolyte lifetime. *return*

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213 *An Investigation of FinFET Single-Event Latch-up Characteristic and Mitigation Method*

Dongqing Li (Institute of modern physics, Chinese Academy of Sci), Tianqi Liu (Institute of modern physics, Chinese Academy of Sci), Zhenyu Wu (National University of Defense Technology), Chang Cai (Institute of modern physics, Chinese Academy of Sci), Peixiong Zhao (Institute of modern physics, Chinese Academy of Sci), Ze He (Institute of modern physics, Chinese Academy of Sci) and Jie Liu (Institute of modern physics, Chinese Academy of Sci).

Abstract

Abstract –FinFET technology compared with planar have an increased sensitivity to single-event latch-up. TCAD simulation demonstrates that the reduction in thickness of shallow trench isolation (STI) and nMOS-to-pMOS lateral spacing will reduce the holding voltage, critical charge and increase the current gain of parasitic CMOS Silicon Controlled Rectifier (SCR). Through circuit analysis, it found that the change of parasitic vertical and horizontal resistance is mainly responsible for aforementioned phenomena. In addition, we found that the common protective measures such as guard rings spacing and epitaxial substrate become increasingly difficult. Based on the current preventive methods, we think that appropriate increasing the width of guard rings or increasing the doping depth of guard rings will improve protection from Single-Event Latch-up (SEL). Moreover, we discuss the feasibility of our methods and verify the effectiveness by TCAD simulation. *return*

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214 *Effect of short-circuit degradation on the remaining useful lifetime of SiC MOSFETs and its failure analysis*

He Du (Aalborg University), Sebastian Letz (Fraunhofer Institute for Integrated Systems and Device Technology), Nick Baker (Aalborg University), Thomas Goetz (Fraunhofer Institute for Integrated Systems and Device Technology), Francesco Iannuzzo (Aalborg University) and Andreas Schletz (Fraunhofer Institute for Integrated Systems and Device Technology).

Abstract

This paper investigates the effect of short-circuit degradation on the remaining useful lifetime of SiC MOSFETs. A different number of repetitive short-circuit events have been introduced into the accelerated power cycling tests to assess the impact. The experimental results indicate a gate degradation with the increasing number of short-circuit repetitions, which leads to higher conduction loss and earlier failure. This hypothesis has been validated by performing lock-in thermography, scanning electron microscopy and focused ion beam. *return*

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215 *A Time-domain Stability Analysis Method for Paralleled LLC Resonant Converter System Based on Floquet Theory*

Hong Li (Beijing Jiaotong University), Xiaheng Jiang (Beijing Jiaotong University), Ying Zou (Beijing Jiaotong University) and Chen Liu (Beijing Jiaotong University).

Abstract

In this paper, a stability analysis method based on Floquet theory is firstly proposed to provide an effective stability analysis method for paralleled LLC resonant converter system. Firstly, the time-domain model of a paralleled LLC resonant converter system is established, then, the stable range of the paralleled LLC resonant converter system can be determined by analysing the eigenvalues of the state transfer matrix based on Floquet theory, which is obtained from the established time-domain model. Finally, a two-stage paralleled LLC resonant converter system controlled by average current mode is taken as an example, the correctness and effectiveness of the proposed stability analysis method based on Floquet Theory is verified by simulation. The proposed stability analysis method can avoid the complex derivation of transfer function and impedance in frequency domain analysis methods. *return*

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217 *Reliability Analysis in GeTe and GeSbTe based Phase-Change Memory 4kb Arrays targeting Storage Class Memory Applications*

Giusy Lama (CEA, LETI, MINATEC Campus, F-38054 Grenoble, France and Univ. Grenoble Alpes, F-38000 Grenoble, France), Guillaume Bourgeois (CEA, LETI, MINATEC Campus, F-38054 Grenoble, France), Mathieu Bernard (CEA, LETI, MINATEC Campus, F-38054 Grenoble, France), Niccolo Castellani (CEA, LETI, MINATEC Campus, F-38054 Grenoble, France), Jury Sandrini (CEA, LETI, MINATEC Campus, F-38054 Grenoble, France), Emmanuel Nolot (CEA, LETI, MINATEC Campus, F-38054 Grenoble, France), Julien Garrione (CEA, LETI, MINATEC Campus, F-38054 Grenoble, France), Marie Claire Cyrille (CEA, LETI, MINATEC Campus, F-38054 Grenoble, France), Gabriele Navarro (CEA, LETI, MINATEC Campus, F-38054 Grenoble, France) and Etienne Nowak (CEA, LETI, MINATEC Campus, F-38054 Grenoble, France).

Abstract

Abstract - In this work, we propose a reliability analysis targeting the evaluation of the suitability of a Phase-Change Memory (PCM) device for Storage Class Memory applications. Thanks to the analysis of programming and endurance characteristics in single devices and 4kb arrays we compare two different GeTe and GeSbTe (αGST) based PCM. The evolution of the phase-change material along cycling is triggered by the analysis of subthreshold characteristics and analytical equations based on experimental data for the description of electrical parameters evolution are given. An extrapolation method to evaluate endurance at more than 10^9 cycles required for SCM is described and applied, showing the intrinsic high endurance capability and suitability for SCM applications of αGST wrt GeTe. *return*

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218 *AC stress reliability study on a novel vertical MOS transistor for non-volatile memory technology*

Jordan Locati (STMicroelectronics), Vincenzo Della Marca (IM2NP), Christian Rivero (STMicroelectronics), Pascal Fornara (STMicroelectronics), Arnaud Regnier (STMicroelectronics), Stephan Niel (STMicroelectronics) and Karine Coulié (IM2NP).

Abstract

Abstract – This paper presents a novel high voltage vertical trench MOS transistor designed to be used in a Non-Volatile Memory (NVM) technology. Physical and electrical measurements are carried out to understand the device behaviour. The comprehension is supported by TCAD simulations. Finally, the AC stress reliability results are reported. *return*

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220 *Single event upset for monolithic 3-D integrated 6T SRAM based on a 22 nm FD-SOI technology: Effects of channel size and temperature*

Junjun Zhang (Institute of Microelectronics of the Chinese Academy of Sciences; the University of Chinese Academy of Sciences), Fanyu Liu (Institute of Microelectronics of the Chinese Academy of Sciences), Bo Li (Institute of Microelectronics of the Chinese Academy of Sciences), Binhong Li (Institute of Microelectronics of the Chinese Academy of Sciences), Yang Huang (Institute of Microelectronics of the Chinese Academy of Sciences), Can Yang (Institute of Microelectronics of the Chinese Academy of Sciences), Guoqing Wang (Institute of Microelectronics of the Chinese Academy of Sciences), Rongwei Wang (Institute of Microelectronics of the Chinese Academy of Sciences), Jiajun Luo (Institute of Microelectronics of the Chinese Academy of Sciences) and Zhengsheng Han (Institute of Microelectronics of the Chinese Academy of Sciences).

Abstract

The single event upset (SEU) for monolithic 3-D (M3D) 6T SRAM with different channel sizes was investigated based on a 22 nm fully-depleted silicon-on-insulator (FD-SOI) technology over a temperature range of 210 K to 390 K. Compared with planar SRAM, M3D SRAM exhibits higher SEU sensitivity and increasing the transistor size does not work in mitigating the SEU in M3D. It is demonstrated that the SEU sensitivity of M3D 6T SRAM increases with temperature after the incident of 127I while it decreases after the striking of 209Bi. The reason can primarily be explained by the different influence ranges of striking heavy ions, which affects the ionized charge transport. *return*

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221 *Reliability of H-terminated diamond MESFETs in high power dissipation operating condition*

Carlo De Santi (University of Padova), Luca Pavanello (University of Padova), Arianna Nardo (University of Padova), Claudio Verona (University of Rome "Tor Vergata"), Gianluca Verona Rinati (University of Rome "Tor Vergata"), Gaudenzio Meneghesso (University of Padova), Enrico Zanoni (University of Padova) and Matteo Meneghini (University of Padova).

Abstract

The aim of this work is to study the catastrophic and gradual degradation of H-terminated diamond MESFETs. They are able to withstand high power densities before failure, but are still affected by a bias-dependent degradation. The main degradation modes are an increase in ON-resistance and threshold voltage, and are caused by the higher concentration of a 0.3 eV deep level. Electroluminescence measurements confirm the increase in electron scattering, and highlight a progressive reduction in peak electric field in the device under test, possibly due to a virtual field plate effect. *return*

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222 *Electro-thermal Evaluation and Comparison of Quasi-Z Source Inverter Using Different Modulation Methods in Wind Power System*

Peng Fan (School of Electrical and Information Engineering, Hunan University, Changsha, China), Shoudao Huang (School of Electrical and Information Engineering, Hunan University, Changsha, China) and Derong Luo (School of Electrical and Information Engineering, Hunan University, Changsha, China).

Abstract

This paper focuses on the thermal loading of the novel quasi Z source inverter based wind power generation system. The lifetime of the wind power converter is strongly influenced by the thermal behaviour of the power devices and their mission profile. For the unique boost modulations of quasi Z

source grid-connected inverter, an electro-thermal model is rebuilt to calculate the semiconductor junction temperature. And a simulation platform is developed in Simulink environment to analyse the electro-thermal dynamics of the system by using different modulation strategies and analysing different wind-load conditions. The results show that power loss in both positive and negative half output cycle will prevent the decline of junction temperature in semiconductor devices. For segment boost modulation, variable wind speed can reduce the temperature fluctuation due to the increasing loss in negative half output cycle. *return*

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223 *Hot-Carrier Degradation in P- and N- Channel EDMOS for Smart Power Application*

Shuang Li (ISEN-IM2NP), Alain Bravaix (ISEN), Edith Kussener (ISEN-IM2NP), David Ney (STMicroelectronics), Xavier Federspiel (STMicroelectronics) and Florian Cacho (STMicroelectronics).

Abstract

P- and N- channel Extended Drain MOSFETs (EDMOS) are analyzed through its sensitivity to Hot-Carrier (HC) degradation using accelerated lifetime technique. We have improved the extraction of series-resistance (dRSD) with a 2nd order mobility modeling applied to HC degradation as a function of stressing VGS from VGS= 0 to VGmax. This allows to determine the worst-case of lifetime dependence in relation to the damage in the drift zone where breakdown sensitivity is found to be intimately bound up with the hot-hole (HH) injection efficiency in N-EDMOS while P-EDMOS exhibits a larger security margin. *return*

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224 *GaN-based high-periodicity multiple quantum well solar cells: degradation under optical and electrical stress*

Alessandro Caria (University of Padova), Carlo De Santi (University of Padova), Filippo Zamperetti (University of Padova), Xuanqi Huang (Arizona State University), Houqiang Fu (Arizona State University), Hong Chen (Arizona State University), Yuji Zhao (Arizona State University), Andrea Neviani (University of Padova), Gaudenzio Meneghesso (University of Padova), Enrico Zanoni (University of Padova) and Matteo Meneghini (University of Padova).

Abstract

We investigate the degradation of InGaN-GaN MQW solar cells under optical and electrical stress. We submitted the devices to high temperature, high optical power stress and we found that, under optical stress, the devices show a moderate decrease in open-circuit voltage, possibly due to creation of defect-related shunt paths. This degradation is partially recovered after room temperature storage. The stronger decrease of open-circuit voltage under electrical stress at high current suggests a role of carrier flow in the degradation. *return*

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225 *New power module concept in PCB-Embedded technology with silver sintering die attach*

Amina Tablati (VEDECOM Institute), Nadim Alayli (VEDECOM Institute), Toni Youssef (VEDECOM Institute), Olivier Belnoue (ELVIA PCB), Loic Théolier (Univ. Bordeaux) and Eric Woirgard (Univ. Bordeaux).

Abstract

This study deals with the reliability of a new power embedded PCB (printed circuit board) concept highly integrated into an electrical machine for aeronautical and automotive applications. The first part describes the assembly topology and presents the main stages of module manufacturing using the silver sintering connection and the pre-impregnated composite fibers lamination. A second part shows the results of electrical and mechanical tests realized on this module. The purpose is to validate the design of a new assembly technology which offers all the reliability conditions that are the manufacturing time optimization, the reduction of the process steps, the module functionality and the feasibility. *return*

226 *Investigation of the Current Collapse behaviour in GaN Power HEMTs with highly adjustable pulse and measurement concept*

Maximilian Goller (Chemnitz University of Technology), Marc André Thim (Chemnitz University of Technology), Jianhua Song (Chemnitz University of Technology), Jens Kowalsky (Chemnitz University of Technology), Jörg Franke (Chemnitz University of Technology) and Josef Lutz (Chemnitz University of Technology).

Abstract

The dynamic RDSon or current collapse of Gallium Nitride (GaN) power HEMT devices was investigated under soft switching operation using a pulse test circuit, based on a half bridge configuration. The presented test and measurement setup allows device operation under adjustable high voltage and current with inexpensive measurement methods. A flexible adaption of the pulse pattern allows operation with and without biasing the device under test with high voltage before the pulse. Hence, the static and dynamic values of the RDSon can be determined in one single test setup under identical conditions and device configuration. Doing so, different stress conditions could be realized including variable drain-source blocking voltage VDS,off for adjustable stress time tstress and temperature ϑ. The results show strong dependency of RDSon on the stress time and the drain-source voltage. Furthermore, indications of a strong influence of the trapping process on dynamic effects as well as an optimal operation for the devices at very low off-state stress times in application are observed.

228 *CFD Modelling of Additive Manufacturing Liquid Cold Plates for More Reliable Power Press-Pack Assemblies*

Paolo Cova (University of Parma), Danilo Santoro (University of Parma), Davide Spaggiari (University of Parma), Federico Portesine (Poseico S.p.A.), Filippo Vaccaro (Poseico S.p.A.) and Nicola Delmonte (Department of Engineering and Architecture - University of Parma).

Abstract

In this work a new concept of liquid cold plate for high power press-pack assemblies is investigated. In industrial applications it is very important to reduce the volume and weight of the device-heatsink stack, in order to improve reliability and availability of the whole system. The potential of aluminum additive manufacturing technology is investigated by means of coupled thermal fluid-dynamic 3D modelling in order to get the best trade-off between thickness, thermal performance, and pressure drop. Careful tuning of the numerical model was conducted by means of thermal characterization of a prototype with a test bench properly built. The numerical model was exploited to explore different solutions for the cold plate internal layout, such as with classical coils, deformed coils, or specific textures impossible with standard mechanical machining. Early results are shown to demonstrate the usefulness of our coupled thermal fluid-dynamic approach. Mechanical analysis was taken into account as well, and will be shown in the full paper. *return*

229 *Impact of Crystalline Orientation of Lead-Free Solder Joints on Thermomechanical Response and Reliability of Ball Grid Array Components*

Emna Ben Romdhane (IRT Saint Exupéry , CS34436, 3 Rue Tarfaya, 31400 Toulouse), Alexandrine Guédon-Gracia (Laboratoire de l'Intégration du Matériau au Système, IMS, UMR 5218, 33405 Talence), Samuel Pin (IRT Saint Exupéry , CS34436, 3 Rue Tarfaya, 31400 Toulouse), Pierre Roumanille (IRT Saint Exupéry , CS34436, 3 Rue Tarfaya, 31400 Toulouse) and Hélène Frémont (Laboratoire de l'Intégration du Matériau au Système, IMS, UMR 5218, 33405 Talence).

Abstract

The microstructure of lead-free solder joints often consists of only one or a few randomly oriented tin grains as a result of conditions and reactions that take place during the solidification. Due to severe anisotropy of tin phase and this complex microstructure, the stress state of each joint will be unique, and lead to a dispersion in times to fail. This study aims at evaluating the impact of orientations of tin grains on

the stress state of a BGA component. Different combinations of solder joint grain orientations are studied through thermo-mechanical simulations in order to assess the stress state of each joint. return

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230 *Analysis of counterfeit electronics*

Giovanna Mura (DIEE- University of Cagliari), Roberto Murru (DIEE- University of Cagliari) and Giovanni Martines (DIEE- University of Cagliari).

Abstract

Counterfeit electronics pose reliability risks and severe harms. The failures of systems that use counterfeits can cause safety and security problems. Many factors contribute: lack of carefulness on the part of buyers, obsolescence, lower prices, costly inspection procedures, absence of origin verification tools. Two case studies are proposed to add a piece of information in this context. They add evidence regarding the capillary penetration of the counterfeit devices. It should contribute to arise some concerns. return

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231 *IGBT Aging Monitoring and Remaining Lifetime Prediction Based on Long Short-Term Memory (LSTM) Networks*

Wanping Li (Xi'an Jiaotong University), Bixuan Wang (Xi'an Jiaotong University), Jingcun Liu (Xi'an Jiaotong University), Guogang Zhang (Xi'an Jiaotong University) and Jianhua Wang (Xi'an Jiaotong University).

Abstract

In this paper, the online aging monitoring system of IGBTs is built and its thermal circuit is carefully designed. A detailed error analysis is conducted on the measurement system, which shows a decent uncertainty of the precursors obtained. Based on the test results, a novel machine learning technique, i.e. recurrent neural networks (RNN) using long short-term memory (LSTM) units, is introduced to predict the remaining lifetime prediction and outperforms the typical extended Kalman filter (EKF). return

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232 *Improving GPU register file reliability with a comprehensive ISA extension*

Marcio Goncalves (Federal University of Rio Grande do Sul (UFRGS)), Josie Esteban Rodriguez Condia (Politecnico di Torino), Matteo Sonza Reorda (Politecnico di Torino), Luca Sterpone (Politecnico di Torino) and Jose Rodrigo Azambuja (Federal University of Rio Grande do Sul (UFRGS)).

Abstract

This work proposes a comprehensive ISA extension to improve GPU reliability to transient effects. Three additional instructions are proposed, implemented, and combined with software-based datapath duplication. Modified program codes are compared to state-of-the-art software-based fault tolerance techniques in terms of execution time, the circuit area is evaluated against the original GPU architecture, and a fault injection campaign is performed to assess reliability. Results show that the proposed ISA extension improves the performance of software-based approaches while maintaining fault detection capabilities at negligible costs in the circuit area. This work can help engineers in designing more efficient and resilient GPU architectures. return

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234 *Non-destructive Automatic Die-Level Defect Detection of Counterfeit Microelectronics using Machine Vision*

Bahar Ahmadi (University of Connecticut), Richard Heredia (Manhattan College), Sina Shahbazmohamadi (University of Connecticut) and Zahra Shahbazi (Manhattan College).

Abstract

Abstract –The goal of this paper is to automate the process of IC counterfeit detection using Non-destructive Imaging Techniques. The defects targeted in this study are the most prevalent die-level defects

with possible multi-dimensional features, making their non-destructive detection challenging. Non-destructive X-ray microtomography is a powerful tool to obtain 3D internal information on microelectronics but usually results in large datasets and a stack of more than a thousand 2D images requiring a subject matter expert to investigate them individually for potential defects. Such a detection method is time-consuming, costly and subjective being largely dependent on the level of expertise, experience, and diligence. Our method addresses those challenges by incorporating machine vision instead of human input for detection. *return*

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237 *Comparing Analytical and Monte-Carlo-based Simulation Methods for Logic Gates SET Sensitivity Evaluation*

Rafael Schvittz (Universidade Federal do Rio Grande), Ygor Quadros Aguiar (Université de Montpellier - IES/RADIAC), Frédéric Wrobel (Université de Montpellier - IES/RADIAC), Jean-Luc Autran (Aix-Marseille Université), Leomar Rosa Jr (UFPel) and Paulo F. Butzen (UFRGS - Brazil).

Abstract

The downscaling of feature sizes increases the susceptibility to Single Event Effects in integrated circuits. As a manner to mitigate soft errors, solutions incur significant performance and area penalties. This paper proposes a discussion about two methods to evaluate gate susceptibility considering Single Event Transient faults at the gate layout level. The results show the need for fast and accurate methods to evaluate logic gates susceptibility to make it possible to evaluate the most reliable option. *return*

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240 *Experimental setup to monitor non-destructive single ionization events caused in power devices by terrestrial cosmic radiation.*

Marco Pocaterra (ETH Zurich, Integrated Systems Laboratory) and Mauro Ciappa (ETH Zurich).

Abstract

A dedicated experimental setup is presented for the acquisition of single ionization events occurring in power devices due to terrestrial cosmic radiation. This spectrometer chain is designed to be used for long-term experiments, where devices are submitted to the natural cosmic radiation, as well as for experiments using radioactive sources, and TCR tests. Every single ionization event that generates in the device charge pulses ranging from 1 fC up to 2 pC is recorded together with its time stamp and waveform. Original pile-up rejection strategies are implemented, which enable to acquire up to 40'000 events per second. The dedicated hardware and software are described in very detail in conjunction with the main operating procedures. Examples are presented, where the ionization events are classified, which occur in a SiC MOSFETs and in a Si Power diode during more than 30'000 hours operation. *return*

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241 *Gate Threshold Voltage Instability and On-resistance Degradation under Reverse Current Conduction Stress on E-mode GaN-HEMTs*

Taichi Nakayama (University of Tsukuba), Tomoyuki Mannen (University of Tsukuba), Akira Nakajima (University of Tsukuba) and Takanori Isobe (University of Tsukuba).

Abstract

This paper investigates the characteristic fluctuation of E-mode GaN-HEMTs, especially focusing under reverse current conduction. The experimental results exhibit that the energy stress of reverse current conduction is relatively higher than that of forward current conduction. After forward and reverse stress, gate threshold voltages were slightly shifted to positive and negative, respectively, which indicates different degradation mechanisms in each case. On the other hand, on-resistances were increased with time duration in the both stress conditions. *return*

242 *Correlative microscopy workflow for precise targeted failure analysis of multi-layer ceramic capacitors*

Nicholas May (University of Connecticut), Joseph Favata (University of Connecticut), Bahar Ahmadi (University of Connecticut), Pouya Tavousi (University of Connecticut) and Sina Shahbazmohamadi (University of Connecticut).

Abstract

Abstract –The correlative framework includes three-dimensional X-Ray tomography, femto-second laser micro machining, three-dimensional FIB/SEM/EDS tomography, and data segmentation. This framework is highly efficient allowing non-destructive locating of the defect and nanometer precise targeting with communication between instruments. The analyses resulted in a fully segmented three-dimensional data set revealing a failure mode of leakage due to suspended metal within the dielectric material. *return*

243 *Gate-damage accumulation and off-line recovery in SiC power MOSFETs with soft short-circuit failure mode*

Alberto Castellazzi (Solid-State Power Processing Lab, Engineering Faculty, Kyoto University of Advanced Science (KUAS)), Frédéric Richardeau (LAPLACE, University of Toulouse, CNRS), Alessandro Borghese (Department of Electrical Engineering and Information technologies University of Naples "Federico II"), Francois Boige (LAPLACE, University of Toulouse, CNRS), Asad Fayyaz (PEMC Group, University of Nottingham), Andrea Irace (Department of Electrical Engineering and Information technologies University of Naples "Federico II"), Gerald Guibaud (ITEC Lab, THALES) and Vanessa Chazal (ITEC Lab, THALES).

Abstract

This paper proposes the detailed analysis of the short-circuit failure mechanism of a particular class of silicon carbide (SiC) power MOSFETs, exhibiting a safe fail-to-open-circuit (also named soft) type signature. The results based on extensive experimental testing, including both functional and structural characterisation of the transistors, specifically devised to bring along gradual degradation and progressive damage accumulation. It is shown that the soft failure feature is associated with degradation and eventual partial shorting of the gate-source structure, Moreover, partial recovery is also observed on degraded components, which can be forced and to some extent controlled by applying specific biasing in off-line conditions, making it a new realistic option for deployment in the application to yield enhanced system level robustness and hopping-home operational mode capability, of great importance in a number of reliability critical domains, such as transportation and energy distribution. *return*

245 *Investigation of Multiple Short-Circuits Characteristics and Reliability in SiC Power Devices used for a Start-up Method of Power Converters*

Tomoyuki Mannen (University of Tsukuba), Takanori Isobe (University of Tsukuba) and Keiji Wada (Tokyo Metropolitan University).

Abstract

This paper investigates characteristics and reliability of SiC power devices used for a start-up method based on multiple short-circuits. A planar-gate and trench-gate SiC-MOSFETs and SiC-JFET employed in a practical power converter are are tested under the start-up method using multiple short-circuits more than 10000 cycles. The experimental results exhibit only the planar-gate SiC-MOSFET can survive the 10000 cycle short-circuit tests with slight degradation under a testing condition. As a result, this paper reveals the planar-gate SiC-MOSFET is suitable for the start-up method due to its characteristic. *return*

246 *Methodology to Evaluate the Critical Blocks in an Integrated Circuit based on the Temperature*

Rafael Nunes (UNICAMP), José Ramirez (UNICAMP) and Roberto Orio (UNICAMP).

Abstract

The increased number of transistors associated with the reduced distance from the transistors and the metal layers raises the maximum chip temperature in the metal lines in each new technology. The high temperature of the chip accelerates the electromigration, increase the resistance of the metal lines, and as a consequence, affect the circuit performance and reliability. The temperature of a block in a chip depends on its power consumption, as also on the power density of the adjacent blocks. Consequently, the floorplan for a given chip can affect the temperature of the chip considerably. In this work, we propose a methodology to evaluate the critical blocks in an integrated circuit based on the temperature and evaluate circuits designed in 45 nm technology. The evaluated circuits have blocks with the temperature above 350 K, and a strategical floorplan is required, as the elevated temperature increases the number of critical lines of the adjacent blocks. The methodology allows the chip floorplanning based on the temperature effects in the resistance increase of the lines due to electromigration. The reduction of the probability of the blocks to failure, and then operates below the maximum temperature supported by the lines can guarantee the circuit reliability. *return*

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248 *Smart Manufacturing through Predictive FA*

Ankush Oberai (Synopsys Inc.) and Rupa Kamoji (Synopsys India Pvt. Ltd.).

Abstract

Goal of the work is a closed loop analysis where FA results are being used in inspection and review steps to improve product yield. Additional rule check is proposed at inline inspection and review step using potential failing patterns from FA. A subset of, machine learning (ML) with image processing and pattern search are used to find the unique patterns of defects by making the machine to build a library (training data) of all failing design structures observed during FA. *return*

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251 *Design of E-Mode GaN HEMTs by the Polarization Super Junction (PSJ) Technology*

Samaneh Sharbati (The Mads Clausen Institute (MCI) , Center for Industrial Electronic (CIE), University of Southern Denmark (SDU)), Thomas Ebel (The Mads Clausen Institute (MCI) , Center for Industrial Electronic (CIE), University of Southern Denmark (SDU)) and Wulf-Toke Franke (The Mads Clausen Institute (MCI) , Center for Industrial Electronic (CIE), University of Southern Denmark (SDU)).

Abstract

Abstract – In this paper, a normally-off high voltage GaN HFETs based on the Polarization Super Junction (PSJ) concept has been presented. In this new device, threshold voltage can be controlled by adjusting the etching depth of the recessed region with remaining on-resistance characteristics. The threshold voltage of E-mode device increased to 2 V while the threshold voltage for experimental D-mode structure was about -4 V. The challenge of achieving high breakdown voltage (BV) with minimum on-resistance has been addressed by the lateral scaling of recessed region to achieve an improved figure of merit (FOM). The specific on-resistance of the proposed E-mode PSJ HFET is maintained low while the BV of the device increases to 800V from 560V of the D-mode PSJ HFET with the same dimensional parameters. *return*

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257 *Parameters sensitivity analysis of Silicon Carbide buck converters to extract features for condition monitoring*

Afshin Loghmani Moghaddam Toussi (Aalborg University), Amir Sajjad Bahman (Aalborg University), Francesco Iannuzzo (Aalborg University) and Frede Blaabjerg (Aalborg University).

Abstract

In this paper the effects of various parameters on the behavior of SiC converters are investigated. SiC devices have many advantages over Si ones; However, they yearn for an increase in their reliability, which can be achieved either by design enhancement or improvement of their corresponding condition

monitoring approaches. The goal here is to replace costly and time-consuming physical experiments with simulations. For the sake of simplicity, we have chosen a buck converter as the testing unit. However, the same approach can be implemented for the other converters. Among the parameters we have investigated are the bond wires, MOSFET parameters, capacitors, and inductors. For these parameters, we have studied how their statistical distributions reproduce the statistical distribution of outputs and also obtained the sensitivities of outputs to them. *return*

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259 *Degradation mechanism of 0.15 um AlGaN/GaN HETMs: the effects of hot electrons*

Zhan Gao (DEI_UNIPD), Fabiana Rampazzo (DEI_UNIPD), Matteo Meneghini (DEI_UNIPD), Carlo De Santi (DEI_UNIPD), Francesca Chiocchetta (DEI_UNIPD), Daniele Marcon (DEI_UNIPD), Gaudenzio Meneghesso (DEI_UNIPD) and Enrico Zanoni (DEI_UNIPD).

Abstract

The degradation mechanisms of AlGaN/GaN HEMTs adopting Fe and C co-doping, with high and low carbon doping concentration was investigated by means of hot-electron step stress and 24 hours' stress tests. Firstly, DC and EL characterization at room temperature are summarized, then the parametric evolution during hot-electron step stress tests at the semi-on state were compared, the assumption for the degradation mechanism is that hot-electrons activated the pre-existing traps in the buffer, attenuate the electric field in the gate drain access region and damaging the gate contact, the parametric evolution during constant stress at (-2 V, 25 V) is discussed. The results further is in accordance with the assumption, proving that the degradation mechanism is hot-electron related. *return*

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260 *A non-invasive SiC MOSFET Junction Temperature Estimation Method based on the Transient Light Emission from the Intrinsic Body Diode*

Giovanni Susinni (University of Catania), Francesco Iannuzzo (University of Aalborg), Angelo Raciti (IMM-CNR) and Santi Agatino Rizzo (University of Catania).

Abstract

A non-invasive temperature sensing method for high-voltage SiC MOSFET chips based on the measurement of light emission during reverse conduction is proposed. The method is based on a fast, inexpensive, simple circuit. The effectiveness of the circuit has been confirmed by the analysis of the transient light emission of intrinsic body diode in a commercial SiC power module. *return*

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262 *Radiation-enhanced glide of 30o Shockley partial dislocations in gallium nitride heterostructures*

Isaak G. Vasileiadis (Physics Department, Aristotle University of Thessaloniki), Imad Belabbas (Université de Bejaia), Joanna Moneta (Institute of High Pressure Physics, Polish Academy of Sciences), Julita Smalc-Koziorowska (Institute of High Pressure Physics, Polish Academy of Sciences), Philomela Komninou (Physics Department, Aristotle University of Thessaloniki) and George P. Dimitrakopulos (Physics Department, Aristotle University of Thessaloniki).

Abstract

The elucidation of core structure of Shockley partial dislocations arising from the dissociation of a-type dislocations in GaN heterostructures, and the study of their behaviour, under electron beam irradiation were the aims of this work. Aberration-corrected high resolution transmission electron microscopy (HRTEM) observations, geometrical phase analysis, image simulations, and density functional theory (DFT) calculations were employed to reveal the dislocation core configurations. Direct visualization of bright atomic columns in the dislocation cores was achieved under optimum imaging conditions allowing for the determination of the core structures. The influence of e-beam irradiation on the partial dislocation mobility in correlation to its core structure was explicitly investigated for a shrinking reaction leading to the merging of a pair of 30o partial dislocations. The role of point defects in the promotion of the re-formation of the

perfect dislocation from the pair of partials was considered. Finally, the impact of this reaction on device performance was considered. *return*

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263 *Study of Moisture Transport in Silicone Gel for IGBT Modules*

Kaichen Zhang (Aalborg University), Gerd Schlottig (ABB Ltd. Corporate Research Center, Switzerland), Elena Mengotti (ABB Ltd. Corporate Research Center, Switzerland), Francesco Iannuzzo (Aalborg University) and Olivier Quittard (ABB Ltd. Semiconductors in Lenzburg, Switzerland).

Abstract

In this paper, an original study on moisture absorption and desorption inside silicone gel for power modules is presented. Silicone gel from two suppliers has been cured at different conditions and exposed to a defined humid environment for a defined period of time. The mass of gel, the relative humidity and the temperature at a certain depth beneath the gel surface have been measured, and a permeability rate of the silicone gels has been calculated. For the two materials we observed significantly different changes in gel mass, but similar humidity levels deep inside the gel. We discuss the influence of curing and bake-out conditions as well as the difference in absorption and transport in the materials. *return*

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264 *Assessing Multi-Output Gaussian Process Regression for Modeling of Non-Monotonic Degradation Trends of Light Emitting Diodes in Storage*

Sze Li Harry Lim (Singapore University of Technology and Design (SUTD)), Pham Luu Trung Duong (Singapore University of Technology and Design (SUTD)), Hyunseok Park (Hanyang University), Preetpal Singh (Chang Gung University), Cher Ming Tan (Chang Gung University) and Nagarajan Raghavan (Singapore University of Technology and Design (SUTD)).

Abstract

Light emitting diodes (LEDs) exhibit different degradation physics under different environmental conditions of humidity, temperature and electrical loading, leading to complex degradation models – a common behavior with several other electronic devices. While most researches focus on degradation under active use, degradation models in storage are often not well established. Large fleet storage of components, in the absence of a degradation model, require laborious continuous inspections despite the preservation under similar environmental conditions. Leveraging on training data from other LEDs within the fleet, stored under similar conditions, this study investigates the utility of multi-output Gaussian Process Regression (MOGPR) with limited test data, to model the complex degradation curve of LEDs in storage, as a proxy for electronic components. We further explore the choice of detrending means and training data sets, to enhance the prediction of degradation curves and residual storage life (RSL). Additional training data sets are observed to give diminishing returns for prediction accuracy. *return*

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265 *Physical Mechanisms for Gate Damages Induced by Heavy Ions in SiC power MOSFET*

Giovanni Busatto (DIEI - University of Cassino and Southern Lazio), Antonio Di Pasquale (DIEI - University of Cassino and Southern Lazio), Daniele Marciano (DIEI - University of Cassino and Southern Lazio), Simone Palazzo (DIEI - University of Cassino and Southern Lazio), Annunziata Sanseverino (DIEI - University of Cassino and Southern Lazio) and Francesco Velardi (DIEI - University of Cassino and Southern Lazio).

Abstract

The objective of the paper is to present a trap assisted tunnel conduction mechanism able to explain the creation of a conductive path in the gate oxide of SiC power MOSFET during the impact of heavy ions. The consequent large current flow through the oxide can induce damages to the gate structure. The model is based on the results of 2D finite element simulation and is supported by previous works dealing with trap assisted tunneling hole injection in silicon dioxide. *return*

IND1 *Electrical nanoprobing and EBIC/EBAC technique integrated in your EFA workflow*

Karl Boche (Imina Technologies SA).

Abstract

Imina Technologies SA is a Swiss manufacturer of robotic solutions for electron and optical microscopes. Its Nanoprobing SEM Solutions set Imina Technologies as a leader in the semiconductor test equipment market for the characterization and failure analysis of microelectronics devices.

The unique motion technology of the miBot™ nanoprober features nanometer positioning resolution, unmatched ease of use and high mechanical stability. The nanoprobing workflow is fully managed using Precisio™, a unified software suite, accelerating the process of establishing steady electrical contacts and acquiring measurements and quantitative data on even the smallest chip technologies. Save, store, sort and synthesize your data in a report with Precisio data management and reporting modules. Join our presentation to have a look at our latest developments, and discover how this intuitive step by step workflow will support you to dramatically reduce your time to data. *return*

IND2 *High Throughput Ultrasonic Inspection Apparatus Using Quasi-static Water Surface Contact*

Natsuki Sugaya (Hitachi Power Solutions Co., Ltd.).

Abstract

Non-destructive testing of semiconductor devices and power modules is indispensable for safety and security society. We have developed high-speed ultrasonic inspection system for 100% inspection using an array transducer with a water fountain. The array transducer performs high-speed inspection by switching the transducer elements sequentially. The quasi-static water film is formed around the elements by the water fountain and contacts to the an inspection surface irradiating ultrasound. This system enables non-immersion inspection by which sample surfaces other than the inspection surface are kept dry. In our presentation, several inspection examples applied this system such as a silicon wafer and an IGBT module are demonstrated. *return*

IND3 *ThermoFisher Static Optical Fault Isolation Roadmap and Lock- In Thermography for Automotive*

Antoine Reverdy (SECTOR TECHNOLOGIES SAS).

Abstract

After a short overview of the ThermoFisher Optical Fault Isolation solutions roadmap focused on static Failure Localization, we will focus on use cases using Lock In Thermography applied to the Automotive Electronics. Nowadays, the automotive market challenges are pushing for fuel efficiency and Advanced Driver Assistance Systems which demand to automotive electronics more complex and sophisticated electronics systems. In the same time, this industry is always expecting to maintain the highest standards of reliability. Considering these two antagonist criteria, most advanced techniques need to be introduce it the reliability/Failure analysis flow to ensure high reliability level of car electronics Two of the main benefits of this technique are the total non destructive approach as well as the real flexibility in term of Device Under Test (from electronic assembly down to single chip). These characteristic make LIT very suitable for the automotive market on which these prerequisites are definitely mandatory. *return*

IND4 *Presentation of the new SMARPROBE LX nanoprober system*

Marc Heinemann (SmarAct GmbH).

Abstract

Due to the ever shrinking size of transistor technology nodes the task of nanoprobing becomes more and more ambitious. Addressing this issue SmarAct GmbH expands the existing SMARPROBE nanoprobing platform with the

new SMARPROBE LX nanoprober, aversatile closed-loop positioning system with an active temperature control and an extended scan range. In this presentation it will be shown how the closed-loop positioning allows the user to position the tips to the point-of-interest in very short time and with as little electron beam exposure as possible. *return*

IND5 *Improved Workflows in Topside and Backside Mechanical Sample Preparation*

Tim Hazeldine (John P. Kummer GmbH).

Abstract

The presentation highlights ULTRA TEC's ASAP-1 IN SITU Mechanical Preparation System that offers through-silicon (RST) thickness mapping and curvature compensation, in a single bench-top footprint. This enables the device to remain mounted throughout processing and measurement, thereby avoiding any potential mounting errors caused during transfer between the prep tool and the microscope. New OVERLAY features allow for X-RAY, C-SAM, mechanical drawings or optical images to be manipulated and locked with the live stage image to enhance the preparation process. *return*

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return to contents

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Li Jing, CN
Li Licheng, CN
Li Qian, CN
Li Shuang, FR
Li Wanping, CN
Li Wenwen, CN
Li Xiang, CN
Li Xiaobing, CN
Li Yaqiu, CN
Li Yongliang, CN
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Lim Sze Li Harry, SG
Lin Li-Hsiang, US
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Ling Sanqiang, CN
Liu Bo, CN
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Liu Datong, CN
Liu Fanyu, CN
Liu Hainan, CN
Liu Heng, CN
Liu Jie, CN
Liu Jingcun, CN
Liu Jinjun, CN
Liu Liansheng, CN
Liu Mingyue, CN
Liu Peiguo, CN
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Lutz Josef, DE
Lv Chunlin, CN

M
Ma Byongjin, KR

return to contents

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Mahmoud Hamouda, CA
Mannen Tomoyuki, JP
Marchand Laurent, NL
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Marcon Daniele, IT
Maresca Luca, IT
Marozau Ivan, CH
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Martines Giovanni, IT
März Martin, DE
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Mastorakis Nikos, GR
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Mateos Javier, ES
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Maures Matthieu, FR
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Meneghesso Gaudenzio, IT
Meneghini Matteo, IT
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Nardo Arianna, IT
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Neviani Andrea, IT
Ney David, FR
Nguyen Tien Anh, FR
Niel Stephan, FR
Ninomiya Tamotsu, JP
Nishizawa Shin-ichi, JP
Niu Hao, CN
Nolot Emmanuel, FR
Nowak Etienne, FR
Nowodzinski Antoine, FR
Nunes Rafael, BR

O
Oberai Ankush, US
Oh Wonwook, KR
Ohguro Tatsuya, JP
Omura Ichiro, JP
Orio Roberto, BR
Orozco Antonio, US
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Ousten Jean-Pierre, FR

P
Palazzo Simone, IT
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Papaioannou George, GR
Park Hyunseok, KP
Patmanidis Konstantinos, AT
Pavanello Luca, IT
Pazos Sebastián Matías, AR
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Peng Yu, CN
Pérez-Martín Elsa, ES
Petit Mickael, FR
Piao Zhelong, CN
Pichon Pierre-Yves, FR
Pin Samuel, FR
Piva Francesco, IT
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Q
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Qiu Dongyuan, CN
Qu Xinpeng, CN
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R
Raciti Angelo, IT
Raghavan Nagarajan, SG
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Regnier Arnaud, FR
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Rey Patrice, FR
Riccio Michele, IT
Richard Isaline, FR
Richardeau Frédéric, FR
Rivero Christian, FR
Rizzo Santi Agatino, IT
Rodriguez Andy, PH
Rodriguez Condia Josie Esteban, CO
Romeo Alessandro, IT
Rosa Jr Leomar, BR
Roumanille Pierre, FR
Rugen Sarah, DE
Rumeau Alexandre, FR
Ruzzarin Maria, IT
Rzepa Gerhard, AT

S
Sagadevan Suresh, MY
Sagné Frédéric, FR
Saito Wataru, JP
Sana Kraiem, TN
Sánchez-Martín Hector, ES
Sandrini Jury, FR
Sangiorgi Enrico, IT
Sanseverino Annunziata, IT
Santoro Danilo, IT
Sapienza Sergio, IT
Sayadi , AT
Scherrer Barbara, CH
Schletz Andreas, DE
Schlottig Gerd, CH
Schneider-Ramelow Martin, DE
Schramm Dorian, BR
Schvittz Rafael, BR
Sciancalepore Corrado, IT
Scognamillo Ciro, IT
Seo Kun Won, KR
Sereda Olha, CH
Shahbazi Zahra, US
Shahbazmohamadi Sina, US
Sharbati Samaneh, DK
Shen Chen, CN
Shim Sunnu, KR
Sicre Sebastien, AT
Sievers Markus, AT
Silber Dieter, DE
Silveira Fernando, UY
Simeu Emmanuel, FR
Simevski Aleksandar, DE
Simonazzi Marco, IT
Singh Preetpal, TW
Smalc-Koziorowska Julita, PL
Soltani Mahdi, DE
Song Jianhua, DE
Song Yuchen, CN
Sonza Reorda Matteo, IT
Soto Frederic, FR
Sozzi Giovanna, IT
Spaggiari Davide, IT
Stampfer Bernhard, AT
Stavrinidis George, GR
Steiner Sebastian, CH
Steinwall Jim, US
Sterpone Luca, IT
Stockman Arno, BE
Stuhldreier Hannes, FR
Sugiyama Masaaki, JP
Sun Qisen, CN
Sun Yongquan, CN
Suñe Jordi, ES
Sung Si-Il, KR
Susinni Giovanni, IT

T
Tablati Amina, FR
Taffarel Mattia, IT
Takamori Taro, JP
Tallarico Andrea Natale, IT
Tan Cher Ming, TW
Tanaka Hideo, JP
Tang Diyin, CN
Tartarin Jean-Guy, FR
Tavousi Pouya, US

Theocharis John, GR
Théolier Loic, FR
Thierry Kociniewski, FR
Thim Marc André, DE
Thomason Mike, US
Tian Guoliang, CN
Toscani Andrea, IT
Touboul Antoine, FR
Trivellin Nicola, IT
Tsao Chun-Cheng, TW
Tsukuda Masanori, JP
Tu Chunming, CN

U Urban Juergen, DE

V Vaccaro Filippo, IT
Van de Casteele Jerome, FR
Van Den Berghe Sebastien, FR
Vanzi Massimo, IT
Vaquero Daniel, ES
Vargas Fabian, BR
Vasileiadis Isaak, GR
Velardi Francesco, IT
Vernica Ionut, DK
Verona Claudio, IT
Verona Rinati Gianluca, IT
Versen Martin, DE
Villiger Thomas, CH
Vinassa Jean-Michel, FR

W Wada Keiji, JP
Wagner Stefan, DE
Waltl Michael, AT
Wan Bo, CN
Wang Bixuan, CN
Wang Boyan, US
Wang Chi-Wei, TW
Wang Chunhui, CN
Wang Chunlin, CN
Wang Dingyi, CN
Wang Guoqing, CN
Wang Haoran, CN
Wang Huai, DK
Wang Jianhua, CN
Wang Puyu, CN
Wang Rongwei, CN
Wang Rui, CN
Wang Shihang, CN
Wang Shujuan, CN
Wang Song, CN
Wang Xiaolin, AU
Wang Xu, CN
Wang Yue, CN
Wang Yujie, CN
Wang Zhian, CN
Waqar Muhammad, KR
Watkins Robert, US
Wei Debao, CN
Wittler Olaf, DE
Woirgard Eric, FR
Won Seokjun, KR
Wong Hiu-Yung, US
Wrobel Frédéric, FR
Wu Jianfei, CN
Wu Kangning, CN
Wu Qinzhi, CN
Wu Ruizhu, GB
Wu Yi-da, US
Wu Zhenyu, CN
Wuest Felix, DE

X Xi Kai, CN
Xiang Zhengrong, CN
Xiao Ming, US
Xin Lei, CN
Xu Gaobo, CN
Xu Jie, CN
Xu Le, CN
Xu Qiuxia, CN
Xu Shukai, CN

Y Yagi Yuki, JP
Yamada Takashi, JP
Yamasue Kohei, JP
Yan Gangping, CN
Yan Xuesong, CN
Yang Can, CN
Yang Guangwen, CN
Yang Guoliang, CN
Yang Jianwei, CN
Yang Jianxiong, CN
Yang Jun, CN
Yang Kexin, US
Yang Pan, CN
Yang Qingqing, CN
Yang Shuying, CN
Yang Xiaofeng, CN
Ye Bing, CN
Ye Shuaichen, CN
Ye Tianchun, CN
Ye Xiaocan, CN
Ye Xuerong, CN
Yin Huaxiang, CN
Yin Jinze, CN
You Shuzhen, BE
Youssef Metayrek, FR
Youssef Toni, FR
Yu Jinsong, CN
Yu Tianhua, CN
Yu Xiaoling, CN
Yu Zechun, DE
Yuan Jiaxin, CN
Yuan Ruiming, CN
Yuan Tao, CN
Yuan Xibo, GB
Yun Ping, CN

Z Zamperetti Filippo, IT
Zanoni , IT
Zanoni Enrico, IT
Zeng Chuanbin, CN
Zhai Guofu, CN
Zhang Bo, CN
Zhang Gang, CN
Zhang Guogang, CN
Zhang Junjun, CN
Zhang Kaichen, DK
Zhang Mengdi, CN
Zhang Sujuan, CN
Zhang Wei, CN
Zhang Xiao-Ping, GB
Zhang Xiaotong, CN
Zhang Xing, CN
Zhang Yan, CN
Zhang Yuhao, US
Zhang Yuna, CN
Zhang Yunan, CN
Zhang Zhen, CN
Zhang Zhixiang, CN
Zhao Dawei, DE
Zhao Fazhan, CN
Zhao Peixiong, CN
Zhao Wenxin, CN
Zhao Xin, CN
Zhao Yongxin, CN
Zhao Yuji, US
Zhao Zhijun, CN
Zheng Trillion Q., CN
Zheng Yifei, CN
Zhou Dao, DK
Zhou Guifa, CN
Zhou Yongliang, CN
Zimmermann André, DE
Zou Ying, CN
Zoubir Khatir, FR

Santorini

return to contents


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